B.S. Abdur Rahman
Crescent
Institute of Science & Technology
Deemed to be University u/s 3 of the UGC Act, 1956

Regulations 2022
Curriculum and Syllabi
(As approved by the 19th Academic Council)
September - 2022

M.Tech.
(VLSI and Embedded System)

B.S. Abdur Rahman Crescent Institute of Science & Technology
Deemed to be University u/s 3 of the UGC Act, 1956
GST Road, Vandalur, Chennai 600 048

REGULATIONS 2022

CURRICULUM AND SYLLABI

(As approved by the 19th Academic Council)

SEPTEMBER – 2022

M.TECH.VLSI AND EMBEDDED SYSTEMS

VISION AND MISSION OF THE INSTITUTION

VISION

B.S. Abdur Rahman Crescent Institute of Science and Technology aspires to be a leader in Education, Training and Research in multidisciplinary areas of importance and to play a vital role in the Socio-Economic progress of the Country in a sustainable manner.

MISSION

- To blossom into an internationally renowned Institute.
- To empower the youth through quality and value-based education.
- To promote professional leadership and entrepreneurship.
- To achieve excellence in all its endeavors to face global challenges.
- To provide excellent teaching and research ambience.
- To network with global Institutions of Excellence, Business, Industry and Research Organizations.
- To contribute to the knowledge base through Scientific enquiry, Applied Research and Innovation.

VISION AND MISSION OF THE DEPARTMENT OFELECTRONICS AND COMMUNICATION ENGINEERING

VISION

The Department of Electronics and Communication Engineering envisions to be a leader in providing state of the art education through excellence in teaching, training, and research in contemporary areas of Electronics and Communication Engineering and aspires to meet the global and socio economic challenges of the country.

MISSION

- The Department of Electronics and Communication Engineering, endeavours to produce globally competent Engineers prepared to face challenges of the society.
- To enable the students to formulate, design and solve problems in applied science and engineering.
- To provide excellent teaching and research environment using state of the art facilities.
- To provide adequate practical training to meet the requirement of the Electronics & communication industry.
- To train the students to take up leadership roles in their career or to pursue higher education and research.

PROGRAMME EDUCATIONAL OBJECTIVES AND OUTCOMES

M.Tech. (VLSI AND EMBEDDED SYSTEM)

PROGRAMME EDUCATIONAL OBJECTIVES:

- **PEO 1:** To design and solve problems in Analog, Digital & Mixed Signal VLSI system design, VLSI Signal Processing, Real Time Embedded System design and Hardware Software Co-Design

- **PEO 2:** To apply the knowledge of software and hardware tools related to the design and implementation of integrated Circuits, Systems for real time embedded applications

- **PEO 3:** To carry out research in various domains and to work in the VLSI and Embedded Systems related industries

- **PEO 4:** To work effectively as a team and manage projects in multidisciplinary environments.

PROGRAMME OUTCOMES:

Graduates will be able to

On successful completion of the programme, the graduates will be able to

- Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- Identify, formulate, research literature, and analyses complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- Use research –based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions.

- Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
- Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

PROGRAMME SPECIFIC OUTCOMES:

Graduates will be able to

- **PSO1**: Be able to analyze, design and implement Analog, Digital and Mixed Signal Circuits and real time embedded systems

- **PSO 2**: Have in-depth knowledge and capability to use industry standard tools in the design and implementation of VLSI and real time Embedded Systems.

- **PSO 3**: Be able to undertake research projects and work as a team in the related domains of VLSI and Embedded systems.

B.S. ABDUR RAHMAN CRESCENT INSTITUTE OF SCIENCE AND TECHNOLOGY, CHENNAI – 600 048.

REGULATIONS 2022

M.Tech. / MCA / M.Sc. / M.Com. / M.A. DEGREE PROGRAMMES

(Under Choice Based Credit System)

1.0 PRELIMINARY DEFINITIONS AND NOMENCLATURE

In these Regulations, unless the context otherwise requires:

i) **"Programme"** means post graduate degree programme (M.Tech. / MCA / M.Sc. / M.Com. / M.A.)

ii) **"Branch"** means specialization or discipline of programme like M.Tech. in Structural Engineering, Food Biotechnology etc., M.Sc. in Physics, Chemistry, Actuarial Science, Biotechnology etc.

iii) **"Course"** means a theory / practical / laboratory integrated theory / mini project / seminar / internship / project and any other subject that is normally studied in a semester like Advanced Concrete Technology, Electro Optic Systems, Financial Reporting and Accounting, Analytical Chemistry, etc.

iv) **"Institution"** means B.S. Abdur Rahman Crescent Institute of Science and Technology.

v) **"Academic Council"** means the Academic Council, which is the apex body on all academic matters of this Institute.

vi) **"Dean (Academic Affairs)"** means the Dean (Academic Affairs) of the Institution who is responsible for the implementation of relevant rules and regulations for all the academic activities.

vii) **"Dean (Student Affairs**)" means the Dean (Students Affairs) of the Institution who is responsible for activities related to student welfare and discipline in the campus.

viii) **"Controller of Examinations"** means the Controller of Examinations of the Institution who is responsible for the conduct of examinations and declaration of results.

ix) **"Dean of the School"** means the Dean of the School of the department concerned.

x) **"Head of the Department"** means the Head of the Department concerned.

2.0 PROGRAMMES OFFERED AND ADMISSION REQUIREMENTS

2.1 Programmes Offered

The various programmes and their mode of study are as follows:

Degree	Mode of Study
M.Tech.	Full Time
MCA	
M.Sc.	
M.Com.	
M.A.	

2.2 ADMISSION REQUIREMENTS

2.2.1 Students for admission to the first semester of the Master's Degree Programme shall be required to have passed the appropriate degree examination as specified in the clause 3.2 [Eligible entry qualifications for admission to programmes] of this Institution or any other University or authority accepted by this Institution.

2.2.2 The other conditions for admission such as class obtained, number of attempts in the qualifying examination and physical fitness will be as prescribed by the Institution from time to time.

3.0 DURATION, ELIGIBILITY AND STRUCTURE OF THE PROGRAMME

3.1. The minimum and maximum period for completion of the programmes are given below:

Programme	Min. No. of Semesters	Max. No. of Semesters
M.Tech.	4	8
MCA	4	8
M.Sc.	4	8
M.Com.	4	8
M.A.	4	8

3.1.1 Each academic semester shall normally comprise of 90 working days. Semester end examinations shall follow within 10 days of the last Instructional day.

3.1.2 Medium of instruction, examinations and project report shall be in English.

3.2 ELIGIBLE ENTRY QUALIFICATIONS FOR ADMISSION TO PROGRAMMES

Sl. No.	Name of the Department	Programmes offered	Eligibility for Admission in M.Tech. / MCA / M.Sc. / M.Com. / MA Programmes
1.	Aeronautical Engineering	M.Tech. (Avionics)	B.E. / B.Tech. in Aeronautical Engineering / Aerospace Engineering / Mechanical Engineering / Mechatronics / EEE / ECE / EIE / or Equivalent degree in relevant field.
2.	Civil Engineering	M.Tech. (Structural Engineering)	B.E. / B.Tech. in Civil Engineering / Structural Engineering or Equivalent degree in relevant field.
		M. Tech. (Construction Engineering and Project Management)	B.E. / B.Tech. in Civil Engineering / Structural Engineering / B.Arch. or Equivalent degree in relevant field.
3.	Mechanical Engineering	M.Tech. (CAD/CAM)	B.E. / B.Tech. in Mechanical / Automobile / Manufacturing / Production / Industrial / Mechatronics / Metallurgy / Aerospace / Aeronautical / Material Science / Polymer / Plastics / Marine Engineering or Equivalent degree in relevant field.
4.	Electrical and Electronics Engineering	M.Tech. (Power Systems Engineering)	B.E. / B.Tech. in EEE / ECE / EIE / ICE / Electronics / Instrumentation Engineering or Equivalent degree in relevant field.
5.	Electronics and Communication Engineering	M.Tech. (VLSI and Embedded Systems)	B.E. / B.Tech. in ECE / EIE / ICE / EEE / IT or Equivalent degree in relevant field.
6.	Computer Science and Engineering	M.Tech. (Computer Science and Engineering)	B.E. / B.Tech. in CSE / IT / ECE / EEE / EIE / ICE / Electronics Engineering / MCA or Equivalent degree in relevant field.
		M.Tech. (Artificial Intelligence and Data Science)	B.E. / B.Tech. in CSE / IT / ECE / EEE / EIE / ICE / Electronics Engineering / MCA or Equivalent degree in relevant field.

Sl. No.	Name of the Department	Programmes offered	Eligibility for Admission in M.Tech. / MCA / M.Sc. / M.Com. / MA Programmes
7.	Information Technology	M.Tech. (Information Technology)	B.E. / B.Tech. in IT / CSE / ECE / EEE / EIE / ICE / Electronics Engineering / MCA or Equivalent degree in relevant field.
8.	Computer Applications	MCA	BCA / B.Sc. Computer Science / B.E. / B.Tech. / B.Sc. Mathematics, B.Sc. Physics / Chemistry / B.Com. / BBA / B.A. with Mathematics at graduation level or at 10 + 2level or equivalent degree in relevant field.
9.	Mathematics	M.Sc. (Actuarial Science)	Any under graduate degree with Mathematics / Statistics as one of the subjects of study at 10 + 2 level.
10.	Physics	M.Sc.(Physics)	B.Sc. in Physics / Applied Science / Electronics /Electronics Science / Electronics & Instrumentation or Equivalent degree in relevant field.
11.	Chemistry	M.Sc.(Chemistry)	B.Sc. in Chemistry / Applied Science or Equivalent degree in relevant field.
12.	Life Sciences	M.Sc. Biochemistry & Molecular Biology	B.Sc. in Biotechnology / Biochemistry / Botany / Zoology / Microbiology / Molecular Biology / Genetics or Equivalent degree in relevant field.
		M.Sc. Biotechnology	B.Sc. in Biotechnology / Biochemistry / Botany / Zoology / Microbiology / Molecular Biology / Genetics or Equivalent degree in relevant field.
		M.Sc. Microbiology	B.Sc.in Biotechnology / Biochemistry / Botany / Zoology / Microbiology / Molecular Biology / Genetics or Equivalent degree in relevant field.
		M.Tech. Biotechnology	B.Tech. / B.E. in Biotechnology or Equivalent degree in relevant field.
		M.Tech. Food Biotechnology	B.E. / B.Tech. in Biotechnology / Food Biotechnology / Chemical Engineering / Biochemical Engineering / Industrial Biotechnology or Equivalent degree in

Sl. No.	Name of the Department	Programmes offered	Eligibility for Admission in M.Tech. / MCA / M.Sc. / M.Com. / MA Programmes
			relevant field.
13.	Commerce	M.Com	B.Com. / BBA
14.	Arabic and Islamic Studies	M.A. Islamic Studies	B.A. in Islamic Studies / Arabic (or) Afzal-ul-Ulama (or) Any under graduate degree with Part 1 Arabic (or) Any under graduate degree with AalimSanad / Diploma / Certificate in Arabic or Islamic Studies.

3.3. STRUCTURE OF THE PROGRAMME

3.3.1 The PG. programmes consist of the following components as prescribed in the respective curriculum:

i. Core courses
ii. Elective courses
iii. Laboratory integrated theory courses
iv. Project work
v. Laboratory courses
vi. Open elective courses
vii. Seminar
viii. Mini Project
ix. Industry Internship
x. MOOC courses (NPTEL- Swayam, Coursera etc.)
xi. Value added courses

3.3.2 The curriculum and syllabi of all programmes shall be approved by the Academic Council of this Institution.

3.3.3 For the award of the degree, the student has to earn a minimum total credits specified in the curriculum of the respective specialization of the programme.

3.3.4 The curriculum of programmes shall be so designed that the minimum prescribed credits required for the award of the degree shall be within the limits specified below:

Programme	Range of credits
M.Tech.	76 - 80
MCA	86
M.Sc.	77 - 85
M.Com.	88
M.A.	72

3.3.5 Credits will be assigned to the courses for all programmes as given below:

- ❖ One credit for one lecture period per week or 15 periods of lecture per semester.
- ❖ One credit for one tutorial period per week or 15 periods per semester.
- ❖ One credit each for seminar/practical session/project of two or three periods per week or 30 periods per semester.
- ❖ One credit for 160 hours of industry internship per semester for all programmes (except M.Com.)
- ❖ Four credits for 160 hours of industry internship per semester for M.Com.

3.3.6 The number of credits the student shall enroll in a non-project semester and project semester is as specified below to facilitate implementation of Choice Based Credit System.

Programme	Non-project semester	Project semester
M.Tech.	9 to 32	18 to 26
MCA	9 to 32	18 to 26
M.Sc.	9 to 32	10 to 26
M.Com.	9 to 32	16 to 28
M.A.	9 to 32	NA

3.3.7 The student may choose a course prescribed in the curriculum from any department offering that course without affecting regular class schedule. The attendance will be maintained course wise only.

3.3.8 The students shall choose the electives from the curriculum with the approval of the Head of the Department / Dean of School.

3.3.9 Apart from the various elective courses listed in the curriculum for each specialization of programme, the student can choose a maximum of two electives from any other similar programmes across departments, aliter to open electives, during the entire period of study, with approval of Head of the department offering the course and parent department.

3.4. ONLINE COURSES

3.4.1 Students are permitted to undergo department approved online courses under SWAYAM up to 40% of credits of courses in a semester excluding project semester (in case of M.Tech. M.Sc. & MCA programmes) with the recommendation of the Head of the Department / Dean of School and with the prior approval of Dean Academic Affairs during his/ her period of study. The credits earned through online courses shall be transferred following the due approval procedures. The online courses can be considered in lieu of core courses and elective courses.

3.4.2 Students shall undergo project related online course on their own with the mentoring of the project supervisor.

3.5 PROJECT WORK

3.5.1 Project work shall be carried out by the student under the supervision of a faculty member in the department with similar specialization.

3.5.2 A student may however, in certain cases, be permitted to work for the project in an Industry / Research organization, with the approval of the Head of the Department/ Dean of School. In such cases, the project work shall be jointly supervised by a faculty of the Department and an Engineer / Scientist / Competent authority from the organization and the student shall be instructed to meet the faculty periodically and to attend the review meetings for evaluating the progress.

3.5.3 The timeline for submission of final project report / dissertation is within 30 calendar days from the last instructional day of the semester in which project is done.

3.5.4 If a student does not comply with the submission of project report / dissertation on or before the specified timeline he / she is

deemed to have not completed the project work and shall re-register in the subsequent semester.

4.0 CLASS ADVISOR AND FACULTY ADVISOR

4.1 CLASS ADVISOR

A faculty member shall be nominated by the HOD/ Dean of School as Class Advisor for the class throughout their period of study.

The class advisor shall be responsible for maintaining the academic, curricular and co-curricular records of students of the class throughout their period of study.

4.2 FACULTY ADVISOR

To help the students in planning their courses of study and for general counseling, the Head of the Department / Dean of School of the students shall attach a maximum of 20 students to a faculty member of the department who shall function as faculty advisor for the students throughout their period of study. Such faculty advisor shall guide the students in taking up the elective courses for registration and enrolment in every semester and also offer advice to the students on academic and related personal matters.

5.0 COURSE COMMITTEE

5.1 Each common theory / laboratory course offered to more than one group of students shall have a “Course Committee” comprising all the teachers handling the common course with one of them nominated as course coordinator. The nomination of the course coordinator shall be made by the Head of the Department / Dean (Academic Affairs) depending upon whether all the teachers handling the common course belong to a single department or from several departments. The Course Committee shall meet as often as possible to prepare a common question paper, scheme of evaluation and ensure uniform evaluation of the assessment tests and semester end examination.

6.0 CLASS COMMITTEE

6.1 A class committee comprising faculty members handling the classes, student representatives and a senior faculty member not handling the courses as chairman will be constituted in every semester:

6.2 The composition of the class committee will be as follows:

i) One senior faculty member preferably not handling courses for the concerned semester, appointed as chairman by the Head of the Department
ii) Faculty members of all courses of the semester
iii) All the students of the class
iv) Faculty advisor and class advisor
v) Head of the Department – Ex officio member

6.3 The class committee shall meet at least three times during the semester. The first meeting shall be held within two weeks from the date of commencement of classes, in which the nature of continuous assessment for various courses and the weightages for each component of assessment shall be decided for the first and second assessment. The second meeting shall be held within a week after the date of first assessment report, to review the students' performance and for follow up action.

6.4 During these two meetings the student members, shall meaningfully interact and express opinions and suggestions to improve the effectiveness of the teaching-learning process, curriculum and syllabi of courses.

6.5 The third meeting of the class committee, excluding the student members, shall meet within 5 days from the last day of the semester end examination to analyze the performance of the students in all the components of assessments and decide their grades in each course. The grades for a common course shall be decided by the concerned course committee and shall be presented to the class committee(s) by the concerned course coordinator.

7.0 REGISTRATION AND ENROLLMENT

7.1 The students of first semester shall register and enroll at the time of admission by paying the prescribed fees. For the subsequent semesters registration for the courses shall be done by the student one week before the last working day of the previous semester.

7.2 Change of a Course

A student can change an enrolled course within 10 working days from the commencement of the course, with the approval of the Dean (Academic Affairs), on the recommendation of the Head of the Department of the student.

7.3 Withdrawal from a Course

A student can withdraw from an enrolled course at any time before the first continuous assessment test for genuine reasons, with the approval of the Dean (Academic Affairs), on the recommendation of the Head of the Department of the student.

7.4 A student can enroll for a maximum of 32 credits during a semester including Redo / Predo courses.

8.0 BREAK OF STUDY FROM PROGRAMME

8.1 A student may be allowed / enforced to take a break of study for two semesters from the programme with the approval of Dean (Academic Affairs) for the following reasons:

8.1.1 Medical or other valid grounds

8.1.2 Award of 'I' grade in all the courses in a semester due to lack of attendance

8.1.3 Debarred due to any act of indiscipline

8.2 The total duration for completion of the programme shall not exceed the prescribed maximum number of semesters (vide clause 3.1).

8.3 A student who has availed a break of study in the current semester (odd/even) can rejoin only in the subsequent corresponding (odd/even) semester in the next academic year on approval from the Dean (Academic affairs).

8.4 During the break of study, the student shall not be allowed to attend any regular classes or participate in any activities of the

Institution. However, he / she shall be permitted to enroll for the 'I' grade courses and appear for the arrear examinations.

9.0 MINIMUM REQUIREMENTS TO REGISTER FOR PROJECT WORK

9.1 A student is permitted to register for project semester, if he/she has earned the minimum number of credits specified below:

Programme	Minimum no. of credits to be earned to enroll for project semester
M.Tech.	18
MCA	22
M.Sc.	18
M.Com	NA
M.A.	NA

9.2 If the student has not earned minimum number of credits specified, he/she has to earn the required credits, at least to the extent of minimum credits specified in clause 9.1 and then register for the project semester.

10.0 ATTENDANCE REQUIREMENT AND SEMESTER / COURSE REPETITION

10.1 A student shall earn 100% attendance in the contact periods of every course, subject to a maximum relaxation of 25% to become eligible to appear for the semester end examination in that course, failing which the student shall be awarded "I" grade in that course.

10.2 The faculty member of each course shall cumulate the attendance details for the semester and furnish the names of the students who have not earned the required attendance in the concerned course to the class advisor. The class advisor shall consolidate and furnish the list of students who have earned less than 75% attendance, in various courses, to the Dean (Academic Affairs) through the Head of the Department / Dean of the School. Thereupon, the Dean (Academic Affairs) shall officially notify the names of such students prevented from writing the semester end examination in each course.

10.3 If a student secures attendance between 65% and less than 75% in any course in a semester, due to medical reasons (hospitalization / accident / specific illness) or due to participation in the institution approved events, the student shall be given exemption from the prescribed attendance requirement and the student shall be permitted to appear for the semester end examination of that course. In all such cases, the students shall submit the required documents immediately after joining the classes to the class advisor, which shall be approved by the Head of the Department / Dean of the School. The Vice Chancellor, based on the recommendation of the Dean (Academic Affairs) may approve the condonation of attendance.

10.4 A student who has obtained an “I” grade in all the courses in a semester is not permitted to move to the next higher semester. Such students shall repeat all the courses of the semester in the subsequent academic year. However, he / she is permitted to redo the courses awarded with 'I' grade / arrear in previous semesters. They shall also be permitted to write arrear examinations by paying the prescribed fee.

10.5 The student awarded “I” grade, shall enroll and repeat the course when it is offered next. In case of “I” grade in an elective course either the same elective course may be repeated or a new elective course may be taken with the approval of the Head of the Department / Dean of the School.

10.6 A student who is awarded “U” grade in a course shall have the option to either write the semester end arrear examination at the end of the subsequent semesters, or to redo the course when the course is offered by the department. Marks scored in the continuous assessment in the redo course shall be considered for grading along with the marks scored in the semester end (redo) examination. If any student obtains “U” grade in the redo course, the marks scored in the continuous assessment test (redo) for that course shall be considered as internal mark for further appearance of arrear examination.

10.7 If a student with “U” grade, who prefers to redo any particular course, fails to earn the minimum 75% attendance while doing

that course, then he / she is not permitted to write the semester end examination and his / her earlier "U" grade and continuous assessment marks shall continue.

11.0 REDO COURSES

11.1 A student can register for a maximum of two redo courses per semester without affecting the regular semester classes, whenever such courses are offered by the department concerned, based on the availability of faculty members, and subject to a specified minimum number of students registering for each of such courses.

11.2 The number of contact hours and the assessment procedure for any redo course shall be the same as regular courses, except there is no provision for any substitute examination and withdrawal from a redo course.

12.0 ASSESSMENT PROCEDURE AND PERCENTAGE WEIGHTAGE OF MARKS

12.1 Every theory course shall have a total of three assessments during a semester as given below:

Assessments	Weightage of Marks
Continuous Assessment 1	25%
Continuous Assessment 2	25%
Semester End Examination	50%

12.2 Theory Course

Appearing for semester end theory examination for each course is mandatory and a student shall secure a minimum of 40% marks in each course in semester end examination for the successful completion of the course.

12.3 Laboratory Course

Every practical course shall have 75% weightage for continuous assessments and 25% for semester end examination. However, a

student shall have secured a minimum of 50% marks in the semester end practical examination for the award of pass grade.

12.4 Laboratory Integrated Theory Courses

For laboratory integrated theory courses, the theory and practical components shall be assessed separately for 100 marks each and consolidated by assigning a weightage of 75% for theory component and 25% for practical component. Grading shall be done for this consolidated mark. Assessment of theory components shall have a total of three assessments with two continuous assessments carrying 25% weightage each and semester end examination carrying 50% weightage. The student shall secure a separate minimum of 40% in the semester end theory examination. The evaluation of practical components shall be through continuous assessment.

12.5 The components of continuous assessment for theory/practical/laboratory integrated theory courses shall be finalized in the first class committee meeting.

12.6 Industry Internship

In the case of industry internship, the student shall submit a report, which shall be evaluated along with an oral examination by a committee of faculty members constituted by the Head of the Department. The student shall also submit an internship completion certificate issued by the industry / research / academic organisation. The weightage of marks for industry internship report and viva voce examination shall be 60% and 40% respectively.

12.7 Project Work

In the case of project work, a committee of faculty members constituted by the Head of the Department / Dean of the School will carry out three periodic reviews. Based on the project report submitted by the students, an oral examination (viva voce) shall be conducted as semester end examination by an external examiner approved by the Controller of Examinations. The weightage for periodic reviews shall be 50%. Of the remaining 50%, 20% shall be for the project report and 30% for the viva voce examination.

12.8 The assessment of seminar course including its component and its weightage shall be decided by a committee of faculty members constituted by the Head of the Department. This committee shall ensure the conduct of assessment of components and award marks accordingly.

12.9 For the first attempt of the arrear theory examination, the internal assessment marks scored for a course during first appearance shall be used for grading along with the marks scored in the arrear examination. From the subsequent appearance onwards, full weightage shall be assigned to the marks scored in the semester end examination and the internal assessment marks secured during the course of study shall become invalid.

In case of laboratory integrated theory courses, after one regular and one arrear appearance, the internal mark of theory component is invalid and full weightage shall be assigned to the marks scored in the semester end examination for theory component. There shall be no arrear or improvement examination for lab components.

13.0 SUBSTITUTE EXAMINATIONS

13.1 A student who is absent, for genuine reasons, may be permitted to write a substitute examination for any one of the two continuous assessment tests of a course by paying the prescribed substitute examination fee. However, permission to take up a substitute examination will be given under exceptional circumstances, such as accidents, admission to a hospital due to illness, etc. by a committee constituted by the Head of the Department / Dean of School for that purpose. However, there is no substitute examination for semester end examination.

13.2 A student shall apply for substitute exam in the prescribed form to the Head of the Department / Dean of School within a week from the date of assessment test. However, the substitute examination will be conducted only after the last working day of the semester and before the semester end examination.

14.0 SUPPLEMENTARY EXAMINATION

14.1 Final Year students can apply for supplementary examination for a maximum of three courses thus providing an opportunity to complete their degree programme. Likewise, students with less credit can also apply for supplementary examination for a maximum of three courses to enable them to earn minimum credits to move to higher semester. The students can apply for supplementary examination within three weeks of the declaration of results in both odd and even semesters.

15. PASSING, DECLARATION OF RESULTS AND GRADE SHEET

15.1 All assessments of a course shall be made on absolute marks basis. However, the Class Committee without the student members shall preferably meet within 5 days after the semester end examination and analyze the performance of students in all assessments of a course and award letter grades. The letter grades and the corresponding grade points are as follows:

Letter Grade	Grade Points
S	10
A	9
B	8
C	7
D	6
E	5
U	0
I	0

"I" denotes inadequate attendance and hence prevented from appearing for semester end examination

"U" denotes unsuccessful performance in the course.

15.2 A student who earns a minimum of five grade points ('E' grade) in a course is declared to have successfully completed the course. Such a course cannot be repeated by the student for improvement of grade.

15.3 The results, after awarding of grades, shall be signed by the Chairman of the Class Committee and Head of the Department/Dean of School and it shall be declared by the Controller of Examinations.

15.4 Within one week from the date of declaration of result, a student can apply for revaluation of his / her semester end theory examination answer scripts of one or more courses, on payment of prescribed fees tothe Controller of Examinations. Subsequently the Head of the Department/ Dean of School offered the course shall constitute a revaluation committee consisting of Chairman of the Class Committee as convener, the faculty member of the course and a senior faculty member knowledgeable in that course as members. The committee shall meet within a week to re-evaluate the answer scripts and submit its report to the Controller of Examinations for consideration and decision.

15.5 After results are declared, grade sheets shall be issued to each student, which contains the following details: a) list of courses enrolled during the semester including redo courses / arrear courses, if any; b) grades scored; c) Grade Point Average (GPA) for the semester and d) Cumulative Grade Point Average (CGPA) of all courses enrolled from first semester onwards.

GPA is the ratio of the sum of the products of the number of credits of courses registered and the grade points corresponding to the grades scored in those courses, taken for all the courses, to the sum of the number of credits of all the courses in the semester.

If C_i, is the number of credits assigned for the i^{th} course and GP_i is the Grade Point in the i^{th} course

$$GPA = \frac{\sum_{i=1}^{n}(C_i)(GPi)}{\sum_{i=1}^{n} C_i}$$

Where n = number of courses

The Cumulative Grade Point Average (CGPA) is calculated in a similar manner, considering all the courses enrolled from first semester.

"I" grade is excluded for calculating GPA.

"U" and**"I"** grades are excluded for calculating CGPA.

The formula for the conversion of CGPA to equivalent percentage of marks is as follows:

Percentage Equivalent of Marks = CGPA X 10

15.6 After successful completion of the programme, the Degree shall be awarded upon fulfillment of curriculum requirements and classification based on CGPA as follows:

Classification	CGPA
First Class with Distinction	8.50 and above and passing all the courses in first appearance and completing the programme within the minimum prescribed period.
First Class	6.50 and above and completing the programme within a minimum prescribed period plus two semesters.
Second Class	Others

15.6.1 Eligibility for First Class with Distinction

- A student should not have obtained 'U' or 'I' grade in any course during his/her study
- A student should have completed the PG programme within the minimum prescribed period of study (except clause 8.1.1)

15.6.2 Eligibility for First Class

A student should have passed the examination in all the courses not more than two semesters beyond the minimum prescribed period of study (except clause 8.1.1)

15.6.3 The students who do not satisfy clause 15.6.1 and clause 15.6.2 shall be classified as second class.

15.6.4 The CGPA shall be rounded to two decimal places for the purpose of classification. The CGPA shall be considered up to three decimal places for the purpose of comparison of performance of students and ranking.

16.0 DISCIPLINE

16.1 Every student is expected to observe discipline and decorum both inside and outside the campus and not to indulge in any activity which tends to affect the reputation of the Institution.

16.2 Any act of indiscipline of a student, reported to the Dean (Student Affairs), through the HOD / Dean shall be referred to a Discipline and Welfare Committee constituted by the Registrar for taking appropriate action.

17.0 ELIGIBILITY FOR THE AWARD OF THE MASTER'S DEGREE

17.1 A student shall be declared to be eligible for the award of the Master's Degree, if he/she has:

i. Successfully acquired the required credits as specified in the curriculum corresponding to his/her programme within the stipulated time.
ii. No disciplinary action is pending against him/her.
iii. Enrolled and completed at least one value added course.
iv. Enrollment in at least one MOOC / SWAYAM course (non-credit) before the final semester.

17.2 The award of the degree must have been approved by the Institute.

18.0 POWER TO MODIFY

Notwithstanding all that have been stated above, the Academic Council has the right to modify any of the above regulations from time to time.

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B.S. ABDUR RAHMAN CRESCENT INSTITUTE OF SCIENCE ANDTECHNOLOGY

M.TECH. VLSI AND EMBEDDED SYSTEMS

CURRICULUM & SYLLABUS, REGULATIONS 2022

SEMESTER I

Sl. No.	Course Code	Course Title	L	T	P	C
1	MAE 6184	Probability and Matrix Theory	3	1	0	4
2	ECE 6121	Digital VLSI Design	3	0	0	3
3	ECE 6122	Advanced Embedded System and Programming	3	0	0	3
4	ECE 6123	Low Power IC Design	3	0	0	3
5	ECE 6124	Embedded Processor Architectures and Programming	3	0	2	4
6	ECE 6125	Digital VLSI Design Laboratory	0	0	2	1
7		Professional Elective (Minimum of 3 credits to be earned)				3
8	ENE 6181	English for Career Development	1	1	0	2
		Credits				**23**

SEMESTER II

Sl. No.	Course Code	Course Title	L	T	P	C
1	GEE 6201	Research Methodology and IPR	2	0	0	2
2	ECE 6221	Real Time Operating Systems	3	0	0	3
3	ECE 6222	Analog Integrated Circuit Design	3	0	2	4
4	ECE 6223	Embedded LINUX	2	0	2	3
5	ECE 6224	Embedded Systems Laboratory	0	0	2	1
6		Professional Elective Courses (Minimum of 9 credits to be earned)				9
		Credits				**22**

SEMESTER III

Sl. No.	Course Code	Course Title	L	T	P	C
1		Open Elective*	3	0	0	3
2		Professional Elective Courses (Minimum of 6 credits to be earned)				6
3	ECE 7121	Industry Internship#				2
4	ECE 7122	Project Work - Phase I	0	0	18	6**
5		MOOC (Related to project)	0	0	0	0
		Credits				**11**

SEMESTER IV

Sl. No.	Course Code	Course Title	L	T	P	C
1	ECE 7122	Project Work - Phase II	0	0	36	18
		Credits				**18 + 6 = 24**

Overall Total Credits: 80

* Open Electives can be chosen from the list, provided that the cumulative credits should not be less than 3.

** Credits for project work phase I in III semester to be accounted along with project work phase II in IV semester

Internship has to be carried out at the end of second semester during summer vacation

LIST OF PROFESSIONAL ELECTIVES- VLSI DESIGN

Sl. No.	Course Code	Course Title	L	T	P	C
1	ECEY 051	CAD for VLSI Circuits	3	0	0	3
2	ECEY 052	ASIC Design	3	0	0	3
3	ECEY 053	Advanced Digital System Design	3	0	0	3
4	ECEY 054	Nano Electronics and Technology	3	0	0	3
5	ECEY 055	CMOS Mixed Signal Circuit Design	3	0	0	3
6	ECEY 056	System Verilog Programming	2	0	0	2
7	ECEY 057	Scripting Languages for VLSI Design Automation	3	0	0	3
8	ECEY 058	RF Integrated Circuit Design	3	0	0	3
9	ECEY 059	Network on Chip	3	0	0	3
10	ECEY 060	SoC Design and Verification	3	0	0	3
11	ECEY 061	Testing of VLSI Circuits	3	0	0	3
12	ECEY 062	VLSI Digital Signal Processing	3	0	0	3

LIST OF PROFESSIONAL ELECTIVES- EMBEDDED SYSTEMS

Sl. No.	Course Code	Course Title	L	T	P	C
1	ECEY 024	Internet of Things	3	0	0	3
2	ECEY 025	Industry 4.0	3	0	2	4
3	ECEY 026	Artificial Intelligence	3	0	0	3
4	ECEY 027	Machine Learning for Embedded Systems	3	0	0	3
5	ECEY 077	Real Time Systems	3	0	0	3
6	ECEY 081	Multicore Architecture	3	0	0	3
7	ECEY 082	Embedded System for Robotics	3	0	0	3
8	ECEY 085	Embedded Automotive Systems	3	0	0	3
9	ECEY 086	Electromagnetic Interference and Compatibility	3	0	0	3

SEMESTER I

MAE 6184	PROBABILITY AND MATRIX THEORY	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

The aim of this course is to impart the

- knowledge of the theory of probability and random variables.
- techniques to carry out probability calculations and identify probability distributions.
- knowledge of the multidimensional random variables.
- familiarizing with the advanced matrix theory concepts.
- importance of variational problems.

PREREQUISITE:

1. Basic concepts of probability, Mutually exclusive events and Independent events.
2. To know to find eigenvalues and eigenvectors of a square symmetric matrix.

MODULE I PROBABILITY AND RANDOM VARIABLE 9+3

Axioms of probability – Addition and Multiplication theorem – conditional probability – Total Probability – Baye's theorem - Random variable – Probability mass function – Probability density functions – Properties – Expectation - Moments – Moments generating functions and their properties.

MODULE II STANDARD DISTRIBUTIONS 9+3

Binomial, Poisson, Geometric, Negative Binomial, Uniform, Exponential, Gamma, weibull and Normal distributions.

MODULE III MULTIDIMENSIONAL RANDOM VARIABLES 9+3

Joint distributions – Marginal and conditional distributions – Covariance – Correlation and Regression - Partial, Multiple correlations and regressions.

MODULE IV ADVANCED MATRIX THEORY 9+3

Matrix norms – singular value decomposition – QR algorithm – pseudo inverse – least square approximations.

MODULE V CALCULUS OF VARIATIONS 9+3

Variation and its properties – Euler's equation – functional dependent on first and higher order derivatives – functional dependent on functions of several independent variables – variational problems with moving boundaries – isoperimetric problems.

L- 45; T-15; TOTAL HOURS - 60

TEXT BOOKS:

1. Sheldon M. Ross, “Introduction to Probability and Statistics for Engineers and Scientists”, Fifth Edition, Elesvier 2016.
2. Richard A. Johnson, “Probability and Statistics for Engineers”, 8th Edition, Pearson Education, 2017.
3. T. Veerarajan, “Probability, Statistics and Random Processes”, 3rd edition, Tata McGraw-Hill Publishing Company Limited, 2008.
4. Lewis D W, “Matrix Theory”, Allied Publishers, Chennai 1995.
5. A. S. Gupta, “Calculus of variations with applications”, PHI Pvt. Ltd. New Delhi 2011.

REFERENCES:

1. H.Cramer, “Random Variables and Probability Distributions”, Cambridge University Press, 2004.
2. S.C.Gupta and V.K.Kapoor, “Fundamentals of Mathematical Statistics”, 12th Edition, Sultan Chand and Sons, 2014.
3. Roger A. Horn, Charles R Johnson , “Matrix Analysis”, Cambridge University Press, 2nd edition, 2012.
4. Elsgolts, “Differential Equations and Calculus of Variations”, University Press of the Pacific, 2003.

COURSE OUTCOMES:

On completion of the course, students will be able to

- do basic problems on probability.
- solve the probability problems using appropriate distributions.
- derive the probability mass / density function of a random variable and multiple correlations and regressions.
- find eigenvalues and eigenvectors of a higher order matrix.
- solve problems of calculus of variations by direct method and using Euler’s formulae.

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

Academic Council:
19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO1 1	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L
CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4 : Quality Education Statement:

SDG 9: Industry, Innovation and Infrastructure.

ECE 6121	DIGITAL VLSI DESIGN	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To discuss the fundamentals of MOS transistors

COB2: To outline the working methodologies of CMOS logic families

COB3: To design a CMOS sub-system circuit to perform a certain functionality with specified speed

COB4: To identify the critical path of a combinational circuit

COB5: To apply pipelining concept in combinational block circuits

PREREQUISITE: Basics of MOSFET, BJT, Digital Electronics

MODULE I THE MOS TRANSISTOR 9

Silicon and Doping, P-N Junction, CMOS Transistor, Threshold Voltage, ON Current, Channel length modulation, Velocity saturation, Sub-threshold leakage, Drain Induced Barrier Leakage, Gate Induced Drain leakage, (Reverse) Short Channel Effect, Other leakage mechanisms, CMOS Inverter - Static Characteristic, Dynamic Characteristic, Introduction to fabrication technologies – crystal growth, Wafer cleaning, Oxidation, Thermal Diffusion, Ion Implantation, Lithography, Epitaxy, Metallization, Dry and Wet etching and Packaging, Fabrication of MOSFET.

MODULE II CMOS LOGIC FAMILIES, COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS 9

Pass Transistors, Transmission Gates; Designing with transmission gates, Primitive Logic Gates; Complex Logic Circuits.SR Latch, clocked Latch and flip flop circuits, CMOS D-latch and edge triggered flip flop - Basic principle, non ideal effects, domino CMOS Logic, high performance dynamic CMOS Circuits, Clocking Issues, Two phase clocking.

MODULE III CMOS SUB SYSTEM DESIGN 9

Data path circuits, Architectures for Adders Full adder circuit design, Inverting Adder, Carry Save Adder, Carry Select Adder, Carry Look Ahead Adder, Accumulators, Multipliers-Basic Terminology, Booth and Modified Booth Encoding, 2s Complement Arithmetic, Array Multiplier, Carry Save Multiplier, Signed multiplication and carry save implementation, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

MODULE IV INTERCONNECT &TIMING METRICS 9

Interconnect Parameters – Capacitance & Timing, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, SelfTimed Circuit Design, Synchronizers and Arbiters, Clock Synthesis and Synchronization Using Phase-Locked Loop.

MODULE V DESIGNING MEMORY AND ARRAY STRUCTURES 9

SRAM and DRAM Memory Core - memory peripheral circuitry - Memory reliability and yield -Power dissipation in memories.

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. Jan M. Rabaey, Anantha Chadrakasan, Borivoje Nikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, PHI, 2016
2. Neil.H, E.Weste, David Harris, Ayan Banerjee, “CMOS VLSI Design: A Circuit and Systems Perspective”, Fourth Edition, Pearson Education, 2011.

REFERENCES:

1. Sorab K Gandhi, “VLSI Fabrication Principles: Si and GaAs”, Second Edition, John Wiley and Sons, 2010.

COURSE OUTCOMES:

On completion of the course, the students will be able to

CO1: classify CMOS fabrication techniques

CO2:design MOSFET based logic circuits

CO3:implement subsystem blocks using CMOS logic

CO4: analyze interconnect and timing issues

CO5:buildmemory peripheral circuits

Board of Studies (BoS) :

23rd BOS of ECE held on 13.07.2022

Academic Council:

19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO1 1	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L
CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4 : Quality Education Statement: The course introduces the IC design with CMOS design techniques, Efficient IC design with less environmental hazards.

SDG 9: Industry, Innovation and Infrastructure,
Statement: Introduce VLSI design with efficient area, timing and power.

ECE 6122	ADVANCED EMBEDDED SYSTEM AND PROGRAMMING	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To explain Embedded system lifecycle and product specification for embedded system

COB2: To discuss Embedded networking protocols

COB3: To apply debugging techniques in embedded IDE

COB4: To analyze the sorting and searching algorithm

COB5: To develop Embedded C and Python programming

PREREQUISITE: Digital Electronics, Microprocessor and Microcontrollers

MODULE I EMBEDDED DESIGN 8

Introduction- Embedded Design life cycle – Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing- Selection Processes – Embedded platform boot sequence- power optimization techniques.

MODULE II EMBEDDED NETWORKING AND INTERRUPTS SERVICE MECHANISM 9

Introduction- I/O Device Ports & Buses– Serial Bus communication protocols - RS232 standard – RS485 –USB – Inter Integrated Circuits (I2C) – CAN bus - interrupt – exception - context switching- interrupt latency and deadline -Introduction to Device Drivers.

MODULE III PROGRAM DESIGN AND ANALYSIS 9

Software Development environment-IDE, assembler, compiler, linker, simulator, debugger, In circuit emulator, Target Hardware Debugging- Process of Assembly linking and Loading- Basic compilation techniques- Program optimization.

MODULE IV EMBEDDED C AND DATA STRUCTURES 10

Introduction to Embedded C –Compare C and Embedded C -Review of data types - Control Structures - Loops - strings and arrays- pointers - functions - Types of Operators- Bitwise Operators - Data structures– Stacks and Queues –-linked list - tree – heap - graph – sorting and searching algorithm.

MODULE V EMBEDDED PYTHON PROGRAMMING 9

Basics of Python – data types- operators- sequential and non-sequential – control statement - functions- module- introduction to SoC – I/O port programming – sensor interfacing with SoC.

L – 45; TOTAL HOURS – 45

TEXT BOOKS:

1. Marilyn Wolf, "Computers as components", Elsevier, 4th edition, 2016.
2. Arnold S. Berger, “Embedded System Design: An introduction to processor,tools and techniques”, CMP books, USA, 2002.
3. Peter Barry, Patrick Crowley, “Modern Embedded Computing” MorganKaufmann Publishers, 2012.

REFERENCES:

1. Michael J Pont, “Embedded C”, Pearson Education, 2007.
2. Jivan S. Parab, Vinod G. Shelake, RajanishK. Kamot, and GourishM.Naik, “Exploring C for Microcontrollers- A Hands on Approach”, Springer, 2007.
3. Mark Lutz, “Learning Python Powerful OOPs”, O’reilly, 2011.

COURSE OUTCOMES:

On completion of the course, the students will be able to

CO1:analyze the quality principles and tools in embedded system during product development process

CO2:design energy efficient embedded systems

CO3:analyze interrupt latency and deadline

CO4:test and debug the coding in embedded systems

CO5:develop software programs to control embedded system using C and Python Languages.

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

Academic Council:
19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO1 1	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	L	L	L	M	M	M	M	M	H	M	L
CO2	H	H	H	H	L	L	L	M	M	M	M	M	M	L	H
CO3	H	H	H	H	L	L	L	M	M	M	M	M	M	L	H
CO4	H	H	H	H	L	L	L	M	M	M	M	M	M	H	L
CO5	H	H	H	H	L	L	L	M	M	M	M	M	M	L	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4 : Quality Education
Statement: The course enhances the programming skills in embedded systems

SDG 9: Industry, Innovation and Infrastructure,
Statement: The course gives an insight to various embedded programming techniques used in industry.

ECE 6123	LOW POWER IC DESIGN	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To describe the power dissipation techniques in CMOS circuits.

COB2: To classify various power optimization techniques.

COB3: To model low power circuits design.

COB4: To analyze the power estimation in CMOS low power circuits.

COB5: To Investigate software design for low power.

PREREQUISITE: Basics of VLSI Design, Analog Electronics

MODULE I POWER DISSIPATION IN CMOS 9

Sources of power dissipation – Physics of power dissipation in MOSFET devices: The MIS structure, long channel MOSFET, Submicron MOSFE, gate induced drain leakage– Power dissipation in CMOS: short circuit dissipation, dynamic dissipation, load capacitance– Low power VLSI design: Limits – principles of low power design, hierarchy of limits, fundamental limit, material limit, device limit, system limit.

MODULE II POWER OPTIMIZATION USING SPECIAL TECHNIQUES 9

Power Reduction in Clock Networks: Clock Gating, Reduced Swing Clock, Oscillator Circuit for Clock Generation, Frequency Division and Multiplication, Other Clock Power Reduction Techniques - CMOS Floating Node: Tristate Keeper Circuit, Blocking Gate, Low Power Bus: Low Swing Bus, Charge Recycling Bus, Delay Balancing - Low Power Techniques for SRAM: SRAM Cell, Memory Bank Partitioning, Pulsed Word line and Reduced bit line Swing.

MODULE III DESIGN OF LOW POWER CIRCUITS 9

Transistor and Gate Sizing : Sizing an Inverter Chain, Transistor and Gate Sizing for Dynamic Power Reduction, Transistor Sizing for Leakage Power Reduction - Network Restructuring and Reorganization : Transistor Network Restructuring, Transistor Network Partitioning and Reorganization - Special Latches and Flip-flops : Self-gating Flip-flop, Combinational Flip-flop, Double Edge Triggered Flip-flop - Low Power Digital Cell Library : Cell Sizes and Spacing, Varieties of Boolean Functions, Adjustable Device Threshold

Voltage.

MODULE IV POWER ESTIMATION 9

Modelling of signals - signal probability calculation - Statistical techniques - estimation of glitching power Sensitivity analysis-Power estimation using input vector compaction, power dissipation in Domino logic, circuit reliability, power estimation at the circuit level, Estimation of maximum power: test generation based approach, steepest descent, generic based algorithm based approach.

MODULE V SOFTWARE DESIGN FOR LOW POWER 9

Sources of software power dissipation - software power estimation: Gate level, architecture level, bus switching activity, instruction level power analysis - software power optimization: minimizing memory access costs, instruction selection and ordering, power management - Automated low power code generation – Co-design for low power.

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2009.
2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995
3. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998

REFERENCES:

1. Dimitrios Soudris, Christians Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002
2. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999
3. AbdelatifBelaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995
4. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, 2001
5. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing Ashok N Kamthane, “Computer Programming”, Pearson Education, 2nd Edition, India, 2012.

COURSE OUTCOMES:

On completion of the course, the students will be able to

CO1: Recall the sources of power dissipation in CMOS.

CO2: Classify the special techniques to mitigate the power consumption in VLSI circuits

CO3: Summarize the power optimization and trade-off techniques in digital circuits.

CO4: Illustrate the power estimation at logic and circuit level

CO5: Apply the software design for low power in various level.

Board of Studies (BoS) :

23rd BOS of ECE held on 13.07.2022

Academic Council:

19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO1 1	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4 :Quality Education

Statement: It is a core course which explains the various low power circuit design which intend to provide quality education.

SDG 9: Industry, Innovation and Infrastructure,

Statement: Low power circuits for modern electronic devices which will enhance quality oflife and to meet industry requirements.

ECE 6124	EMBEDDED PROCESSOR ARCHITECTURES AND PROGRAMMING	L	T	P	C
SDG: 4,9		3	0	2	4

COURSE OBJECTIVES:

COB1: To explain Microcontroller based system design, applications.

COB2: To develop I/O interfaces in system Design.

COB3: To outline about design and programming of MSP 430 microcontroller.

COB4: To choose the ARM architectures and learn various programming techniques.

COB5: To assess practice on workbench /software tools/ hardware processor boards with the supporting Peripherals.

PREREQUISITE: Basics of processor design

MODULE I PIC MICROCONTROLLER ARCHITECTURE 9

Architecture – memory organization – addressing modes –Overview instruction set -I/O ports-bank switching, I/O programming-Timer programming- ADC, DAC and Sensor interfacing, Practice in MPLAB compiler.

MODULE II MSP430 ARCHITECTURE AND PROGRAMMING 9

Architecture – CPU features – Memory structure - Addressing modes – Instruction sets Interrupts programming– Input and Output programming– On-chip peripherals– Flash memory – Low power design-Practice in IAR workbench.

MODULE III ARM ARCHITECTURE AND PROGRAMMING 9

ARM Architecture-LPC2148- The ARM Programmer's model - Instruction set – Thumb instruction set – I/O Programming –UART programming- ADC-DAC-I2C programming-Bit manipulation and Bit Shifting –USB communication.

MODULE IV ARM CORTEX M3 9

Overview of the Cortex-M3- Registers- Special Registers- Instruction Sets- Memory Systems- programming on- chip peripherals.

MODULE V SYSTEM DESIGN – CASE STUDY 9

Interfacing LCD Display – Keypad Interfacing - Motor Control – Controlling DC/ AC appliances – Stand-alone Data Acquisition System.

PRACTICALS **30**

List of Experiments

1. PIC Microcontroller based Assembly / C language programming – Arithmetic Programming in MPLAB compiler.
2. Programming on chip timer of PIC Microcontroller
3. Flashing LED using MSP430 Microcontroller
4. Embedded C -Port programming- Bit manipulation and shifting-UART programming ARM 7–Practice in keil ARM.
5. Assembly/Embedded C programming -On chip peripherals ARM Cortex

L – 45 ; P – 30 ; TOTAL HOURS – 75

TEXT BOOKS:

1. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey “PIC Microcontroller and Embedded Systems using Assembly and C for PIC18”, Pearson Education, 2008.
2. John Iovine, “PIC Microcontroller Project Book”, McGraw Hill, 2000.
3. Rajkamal, “Microcontrollers Architecture, Programming”,Interfacing& System Design”, Pearson, 2012 .
4. Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 3rd Edition, 2014.

REFERENCES:

1. Chris Nagy, “Embedded systems design using the TI MSP430 series”, Elsevier, 2003.
2. Steve Furber, ARM System on Chip Architecture, Addison –Wesley Professional, 2014.

COURSE OUTCOMES:

On completion of the course, the students will be able to

CO1: build ALP and C programs to develop applications using 8051 & PIC Microcontroller.

CO2: examine the embedded programs under KEIL µvision and MPLAB IDE

CO3: uutline the architecture of MSP series of microcontroller.

CO4: demonstrate ALP and C programs to develop applications using the MSP430 Microcontroller.

CO5: design the internal and External IOs of PIC, MSP and ARM processor.

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

Academic Council:
19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4 :Quality Education
Statement: The architectural features for various embedded processors are introduced

SDG 9: Industry, Innovation and Infrastructure,
Statement: Interfacing of external peripherals are studied with embedded processors to expand their applications

ECE 6125	DIGITAL VLSI DESIGN LABORATORY	L	T	P	C
SDG: 4,9		0	0	2	1

COURSE OBJECTIVES:

COB1: To experiment designing with FPGA based digital systems.

COB2: To analyze the performance of the digital systems using EDA tools.

COB3: To develop hands-on experience on the VLSI physical design tools.

COB4: To identify different programming techniques in Verilog HDL

COB5: To compare area, timing and power analysis techniques in Cadence/Tanner.

PREREQUISITE:

Basic knowledge on Digital Electronics, Memory Devices & Verilog Programming.

FPGA BASED EXPERIMENTS:

1. Simulation of sequential and combinational circuits using Verilog HDL.
2. Simulation of Data path circuits and Controller architectures using Verilog HDL.
3. Synthesis of Verilog codes for sequential and combinational circuits on FPGA kits.
4. Development of IP for DSP application.
5. Real time application design using FPGA kit.

ASIC BASED EXPERIMENTS:

6. Standard cell based ASIC RTL realization using Cadence/Tanner.
7. Static and dynamic power Analysis using Cadence/Tanner.
8. Static and dynamic Timing analysis procedures and constraints using Cadence/Tanner.
9. Critical path considerations using Cadence/Tanner.
10. Layout design, LVS, Back annotation using Cadence/Tanner.

P- 30 ; TOTAL HOURS - 30

COURSE OUTCOMES:

On completion of the course, the students will be able to

CO1: To model digital circuits using Verilog HDL.

CO2: Examine and analyze the static and dynamic power of a digital system using EDA tools.
CO3: Inspect and analyze the timing performance of a digital system using EDA tools.
CO4: Identify digital systems satisfying the functionality, timing and power constraints using EDA tools.
CO5: Construct layouts and schematic of digital circuit using EDA .

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

Academic Council:
19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H

Note: L - Low Correlation M - Medium Correlation H - High Correlation

SDG 4 :Quality Education
Statement: To develop optimized hardware design in FPGA used in reconfigurable processors.

SDG 9: Industry, Innovation and Infrastructure,
Statement: ASIC designs are introduced to get a hands on training to design custom made designs in VLSI.

ENE 6181	ENGLISH FOR CAREER DEVELOPMENT	L	T	P	C
SDG: 4 , 8		1	1	0	2

COURSE OBJECTIVES:

COB1: To enable students to learn about the job search, application, and interview process

COB2: To give them an opportunity to explore their global career path, build vocabulary and improve language skills to achieve professional goals

COB3: To produce a professional-looking resume

COB4: To understand networking and interview skills

COB5: To understand the key skills and behaviors required to facilitate a group discussion

Pre-requisites:

The students should have completed a course on English at their Undergraduate level.

MODULE I ENTERING THE JOB MARKET 3+2

Introduction to the Career Development -Job Search Overview-Identifying Your Interests and Skills

Language Focus: Vocabulary and Word Forms Related to Jobs-Choosing the Job that's the Best Fit

Language Focus: Verb Tenses (Present vs. Present Progressive) Understanding Job Descriptions: Reading a Job Advertisement

Language Focus: Phrases to Compare Similarities

Online Learning Opportunities to Extend Your Skills

MODULE II RESUMES 3+2

What is a resume? Why do you need one?

Parts of a Resume-Writing a Resume, Part 1: Name and Contact Information Listening: Connecting Employers with Job Seekers in Today's Economy

Language Focus: Key Words

Writing a Resume, Part 2: Headline and Summary

Writing a Resume, Part 3: Work Experience

Writing a Resume, Part 4: Education

Language Focus: Action Verbs

Writing a Resume, Part 5: Complete your Resume

MODULE III WRITING A COVER LETTER 3+2

What is a Cover Letter?
Professional Writing: Letter Format
Cover Letter: Paragraph 1- Introducing Yourself
Cover Letter: Paragraph 2- Highlighting Your Skills in the Cover letter
Cover Letter: Paragraph 3- Closing
Language Focus – Present Perfect vs. Past Tense
Professional Writing: Level of Formality
Language Focus: Using Modal Verbs to Write politely
Writing a Cover Letter for a Specific Job

MODULE IV INTERVIEWING FOR A JOB 3+5

Overview of the Job Interview: Answering Typical Interview Questions Language Focus: Asking for Clarification in an Interview-
Sample Interview: Do's and Don'ts Part 1
Sample Interview: Do's and Don'ts Part 2
Sample Video: Responding to an Interview Question

MODULE V GROUP DISCUSSION 3+4

Introduction to Group Discussion - Participating in group discussions – understanding group dynamics - brainstorming the topic - questioning and clarifying - GD strategies-activities to improve GD skills

L-15;T-15;TOTAL HOURS - 30

REFERENCES:

1. R. Byrne, D. Teaching Oral Skill. London: Longman. 1975.
2.Byrne, D.Teaching Writing, London: Longman. 1975.
3. Rani Asoka, DeviVimala. English for Career development: ACourse in Functional English. Orient Longman Pvt. Ltd., India,2004.
4. Anderson, K., Maclean, J. & Lynch, T. Study speaking: A Course in Spoken English for Academic Purposes. Cambridge University Press, UK, 2004.
5.Withrow, J., Brookes, G.& Cummings, M.C.Inspired to write. Reading and Tasks to Develop Writing Skills. Cambridge University Press, U.K., 2004.

COURSE OUTCOMES:

CO1: Identify the steps in the job search process

CO2: Describe themselves and their experiences in a résumé

CO3: Build their job-related vocabulary

CO4: Write a clear cover letter that tells employers why they are the right person for the job

CO5: Take part in Group discussion confidently.

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CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H

Note: L - Low Correlation M - Medium Correlation H - High Correlation

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all

SDG 8: Promote sustained, inclusive and sustainable economic growth, full and productive employment and decent work for all

Statement: This course ensures that the students acquire quality education and are also made eligible to obtain productive and decent employment.

SEMESTER II

GEE 6201	RESEARCH METHODOLOGY AND IPR	L	T	P	C
SDG: 4,8,9		2	0	0	2

COURSE OBJECTIVES:

COB1: To apply a perspective on research

COB2: To analyze the research design, information retrieval and problem formulation techniques.

COB3: To select the appropriate statistical techniques for hypothesis construction and methods of data analysis and interpretation

COB4: To execute the effective communications of research findings and apply the ethics in research

COB5: To describe the research findings as research reports, publications, copyrights Patenting and Intellectual Property Rights.

PREREQUISITE:

- Basics of core engineering, probability and statistics.
- Basics of flowchart and algorithm techniques.

MODULE I RESEARCH PROBLEM FORMULATION AND RESEARCH DESIGN 6

Research - objectives – types - Research process, solving engineering problems-Identification of research topic - Formulation of research problem, literature survey and review. Research design - meaning and need - basic concepts - Different research designs, Experimental design - principle, Design of experimental setup, Mathematical modelling - Simulation, validation and experimentation.

MODULE II DATA COLLECTION, ANALYSIS AND INTERPRETATION OF DATA 8

Sources of Data, Use of Internet in Research, Types of Data - Research Data Processing and analysis - Interpretation of results- Correlation with scientific facts - repeatability and reproducibility of results - Accuracy and precision –limitations, Application of Computer in Research- Spreadsheet tool-Basic principles of Statistical Computation. Importance of statistics in research - Concept of probability - Popular distributions - Sample design. Hypothesis testing, ANOVA, Design of experiments - Factorial designs - Orthogonal arrays.

MODULE III OPTIMIZATION TECHNIQUES 8

Use of optimization techniques - Traditional methods – Evolutionary Optimization Techniques. Multivariate analysis Techniques, Classifications, Characteristics, Applications - correlation and regression, Curve fitting.

MODULE IV THE RESEARCH REPORT 8

Purpose of written report - Audience - Synopsis writing - preparing papers for International Journals, Software for paper formatting like LaTeX/MS Office, Reference Management Software, Software for detection of Plagiarism –Thesis writing, - Organization of contents - style of writing-graphs, charts and Presentation tool - Referencing, Oral presentation and defence - Ethics in research - List of funding agencies - scope for research funding - Patenting, Intellectual Property Rights.

L – 30 ; TOTAL HOURS – 30

TEXT BOOKS:

1. Ganesan R, “Research Methodology for Engineers”, MJP Publishers, Chennai, 2011.
2. George E. Dieter, “Engineering Design”, McGraw Hill – International edition, 2020.
3. Kothari C.R, “Research Methodology” – Methods and Techniques, New Age International (P) Ltd, New Delhi, 2020.
4. Kalyanmoy Deb, “Genetic Algorithms for optimization”, Kangal report, No.2001002.

REFERENCES:

1 Holeman, J.P, ”Experimental methods for Engineers”, Tata McGraw Hill Publishing Co., Ltd., New Delhi, 2017.
2 Govt. of India, ”Intellectual Property Laws; Acts, Rules & Regulations”, Universal Law Publishing Co. Pvt. Ltd., New Delhi 2020.
3 R Radha Krishnan & S Balasubramanian, ”Intellectual Property Rights”. 1st Edition, Excel Books, 2012.
4 Derek Bosworth and Elizabeth Webster. ”The Management of Intellectual Property”, Edward Elgar Publishing Ltd., 2013.

COURSE OUTCOMES:

On completion of the course, the students will be able to

CO1: Formulate the research problem

CO2: Design and Analyze the research methodology

CO3: Apply statistical techniques for hypothesis construction

CO4: Analyze and interpret the data to construct and optimize the research hypothesis

CO5: Report the research findings as publications, copyright, trademarks and IPR

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CO1	H	H	H	H	M	L	L	L	L	L	L	L	H	H	H
CO2	H	H	H	H	M	-	-	-	-	-	-	-	H	H	H
CO3	H	H	H	H	M	L	L	L	L	L	L	-	H	H	H
CO4	H	H	H	H	M	-	M	M	M	M	M	-	H	H	H
CO5	H	H	H	H	M	-	M	M	M	M	M	-	H	H	H

Note: L - Low Correlation M - Medium Correlation H - High Correlation

SDG 4: Analysis and design of core field design promotes engineering skills and quality education.

Statement: This course enables the student to analyze the existing technology for further solution and its qualitative measures in terms of societal requirements..

SDG 8: Development of new technologies with core field design provides sustainable economic growth and productive employment.

Statement: To apply the hybrid techniques and concepts for different applications provides sustainable economic growth and productive employment.

SDG 9: Creative and curiosity of core field design fosters innovation and sustainable industrialization.

Statement: This course plays major roles through innovative ideas in industry towards modern infrastructures and sustainability.

ECE 6221	REAL TIME OPERATING SYSTEMS	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To outline the concepts of Operating systems and Real-time Operating Systems

COB2: To analyze the concepts of Resource sharing.

COB3: To discuss the kernel architecture of µC/OS-II RTOS

COB4: To compare various RTOS

COB5: To develop environment to work in real time operating systems

PREREQUISITE:

Concepts of Operating systems, Applications of real time systems

MODULE I REVIEW OF OPERATING SYSTEMS 9

Introduction- operating system services and structures-system calls- process management-process synchronization-classical synchronization problem-CPU scheduling.

MODULE II REAL TIME OPERATING SYSTEM AND SCHEDULING 9

Real-time System-Basic model-characteristics-safety, reliability-types-Timing constraints-Real time task scheduling-classification-clock driven-hybrid schedulers-Event driven scheduling –EDF –RMA-issues.

MODULE III IPC in RTOS 9

Resource sharing –priority inversion-priority inheritance protocol-Highest Locker Protocol-Priority Ceiling Protocol-different types of priority inversions under PCP Feature-issues in IPC protocol-Handling Task Dependencies

Module IV µC/OS-II RTOS 9

Introduction – Features-Kernel Structures- Task Management – Time Management- Event Control Block- Semaphores- Memory Management- Porting RTOS

MODULE V Commercial RTOS and application 9

Comparison and study of various RTOS –VRTX-QNX – VX works – RT Linux Case studies-RTOS for fault Tolerant Applications – RTOS for Control Systems.

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. Rajib Mall, “Real-Time Systems: Theory and Practice”, Pearson, 2009
2. Raj Kamal, “Embedded Systems- Architecture, Programming and Design”, Tata McGraw Hill, 2006.
3. Jane W.S.Liu, “Real Time Systems”, Pearson Education, Asia, 2001.

REFERENCES:

1. Silberschatz, Galvin, Gagne, “Operating System Concepts”, 6th edition, John Wiley, 2003.
2. D.M.Dhamdhere, “Operating Systems, A Concept-Based Approach”, TMH, 2008.
3. Charles Crowley, “Operating Systems-A Design Oriented approach”, Tata McGraw Hill,1996.

COURSE OUTCOMES:

On completion of the course, the students will be able to

CO1: Illustrate OS structure and process scheduling types.

CO2:compare the features of traditional OS and RTOS.

CO3:describe inter task communication and synchronization mechanisms

CO4:analyze and design real time scheduling algorithms

CO5: choose appropriate RTOS for the real time application.

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23rd BOS of ECE held on 13.07.2022

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CO1	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H

Note: L - Low Correlation M - Medium Correlation H - High Correlation

SDG 4 : Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement: Real-time operating system knowledge will provide useful information for high-quality education.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation

Statement : able to advance industrialization through the use of real-time operating system concepts.

ECE 6222	ANALOG INTEGRATED CIRCUIT DESIGN	L	T	P	C
SDG: 4,9		3	0	2	4

COURSE OBJECTIVES:

COB1: Introduce the principles of analog circuits and apply the techniques for the design of analog integrated circuits

COB2: Impart design, and applications of modern analog circuits using CMOS technologies

COB3: Analyze of CMOS Amplifiers and implement a complete analog system.

COB4: To learn about the high-performance Operational amplifiers.

COB5: To impart knowledge on Switched capacitor circuits.

PREREQUISITE: Basics knowledge of Electronic Circuits, VLSI Design, CMOS technology

MODULE I INTRODUCTION TO ANALOG DESIGN 9

Introduction to analog design, MOS device models – MOS Device Layout, MOS Device Capacitance, MOS Small-Signal Model, NMOS vs PMOS devices, Long Channel Vs Short Channel devices, behaviour of MOS as a capacitor.

MODULE II SINGLE STAGE CMOS AMPLIFIERS 9

Basics of single-stage CMOS amplifiers and frequency response - common source, common gate and source follower, passive and active current mirrors.

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MODULE III CMOS DIFFERENTIAL AMPLIFIERS 9

CMOS Operational Amplifiers- one stage and two-stage op-amps - Gain boosting, Common Feedback- Cascode and Folded cascade structures.

MODULE IV HIGH PERFORMANCE OP-AMPS 9

High speed/high-frequency op-amps, micro power op-amps, low noise op-amps and low voltage op-amps, Current mirrors, filter implementations, Supply independent and temperature-independent references, band-gap references, PTAT current generation and constant Gm biasing – CMOS comparators – Multipliers and wave shaping circuits.

MODULE V SWITCHED CAPACITOR CIRCUITS 9

Introduction to switched capacitor circuits, general considerations, sampling switches, switched-capacitor amplifiers, switched-capacitor integrators, switched capacitor common-mode feedback.

PRACTICALS 30

List of Experiments:

1. Verification of MOS Device Characterization and parametric (PAR) analysis
2. Current Mirrors: Simple, cascode, feedback and low-voltage.
3. Simulation of Single stage Amplifiers-Diode connected, Current Mirror Load, PMOS with self-biased load and self-biased CMOS.
4. Characteristics of Simple and cascode current mirror using differential Amplifiers
5. Verification of switched capacitor circuits

L –45 ; P – 30: TOTAL HOURS –75

TEXT BOOKS:

1. David. A. Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley and Sons, 2016
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuit”, Tata McGraw HILL, 2017.

REFERENCES:

1. Philip Allen & Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2013.
2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley Publishers, Fifth Edition, 2009.

COURSE OUTCOMES:

On completion of the course, the students will be able to

CO1: characterize the MOSFET and parametric analysis for the simple MOS models.

CO2: categorize the design of MOSFET based amplifier circuits.

CO3: compare and analyze band gap reference biasing sources.

CO4: distinguish various operational amplifiers and switched capacitor-based circuits.

CO5: evaluate analog integrated circuits using CAD tools.

Board of Studies (BoS) :
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19th Academic Council held on 29.09.2022

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CO1	H	H	H	H	H	L	L	L	M	M	M	M	H	H	H
CO2	H	H	H	H	H	L	L	L	M	M	M	M	H	H	H
CO3	H	H	H	H	H	L	L	L	M	M	M	M	H	H	H
CO4	H	H	H	H	H	L	L	L	M	M	M	M	H	H	H
CO5	H	H	H	H	H	L	L	L	M	M	M	M	H	H	H

Note: L - Low Correlation M - Medium Correlation H - High Correlation

SDG 4: Quality Education.
Statement: It is a core course that explains the various analog integrated circuit design which intend to provide quality education.

SDG 9: Industry, Innovation and Infrastructure
Statement: This course will deliver the concepts to design and innovate analog integrated circuits for modern electronic devices which will enhance quality of life and to meet industry requirements.

ECE 6223	EMBEDDED LINUX	L	T	P	C
SDG: 4,9		2	0	2	3

COURSE OBJECTIVES:

COB1: To describe the architecture of Linux OS, Embedded Linux systems and Command set

COB2: To develop the booting sequence of an Embedded Linux system

COB3: To develop the device driver for Embedded Linux .

COB4: To infer the tool chain and cross compile tool chain in Linux

COB5: To examine hardware emulators QEMU and Linux build environment

PREREQUISITES : Embedded system, Operating system concepts.

MODULE I LINUX FUNDAMENTALS **8**

Linux Community - Desktop vs Embedded - Desktop Linux - Different Linux flavors - Basic Linux Commands - Embedded Linux Basics - Architecture - Hardware Interfaces Supported - Development languages and tool - Host target development setup - Real-time Linux

MODULE II KERNEL INITIALIZATION & DEVICE HANDLING **7**

Embedded Linux Kernel Overview - Kernel Configuration - Compiling The Kernel - Communication between kernel and user space - The Linux Boot Process - The Root File system – Boot loaders In Embedded Linux - Porting Of Linux

MODULE III LINUX DRIVERS & HARDWARE EMULATORS **8**

Introduction to device drivers - Basic components of device drivers - Understandings Needed To Develop A Device Driver - Structure Of Device Driver - __init and __exit attributes - Hardware emulator – QEMU

MODULE IV BUILDING CUSTOM LINUX IMAGE - YOCTO **7**

Building Custom Linux Images - Yocto Project - Poky Distribution - Bitbake and commands -Recipes - meta-Layers - Build directory - Adding Layers and Image configurations - Adding Custom application on Core Image Minimal Build

PRACTICALS **30**

1. To install a virtual box and add Ubuntu 18 OS to the virtual box hosted on a windows machine.
2. To flash the Raspbian image into the SD card and boot the raspberry pi 4 -
    a. Execute the Linux commands for the file system
    b. Execute the Linux command to see the running process in raspberry pi
    c. Execute the Linux command to see the eMMC partition utilization on raspberry pi
3. Develop a Linux device driver for any simple module of your interest and add it to the raspberry pi file system
4. Using the git command fetch the yocto build environment for NXP i.Mx 8 on the ubuntu machine.
5. Write a hello_world.cpp, add it to the environment, build a core-image minimal and visualize the output using QEMU

L – 30 ; P – 30 ; TOTAL HOURS – 60

TEXT BOOKS:

1. Karim Yaghmour, Jon Masters, Gillad Ben Yossef, Philippe Gerum, “Building Embedded linux systems”, O'Reilly, 2008.
2. P. Raghavan, Amol Lad, Sriram Neelakandan, “Embedded Linux System Design and Development”, Auerbach Publications, Taylor and Francis Group, 2006.
3. Craig Hollabaugh, “Embedded Linux : Hardware, Software, and Interfacing”, Addison-Wesley, 2002.

REFERENCES:

1. Karim Yaghmour, “Building Embedded Linux Systems”, O'Reilly & Associates, 2008.
2. MX Yocto Project User's Guide - Rev. LF5.15.32_2.0.0 — 12 July 2022.

COURSE OUTCOMES:

At the end of the course student will able to

CO1: explain about Linux and embedded Linux

CO2:classify the different Linux commands

CO3:interpret the kernel, boot loaders and development of the kernel device driver

CO4: analyze the different cross compile tool chains

CO5:design and develop custom embedded linux applications

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CO2	M	H	L	L	M	L	L	M	M	L	L	L	M	M	H
CO3	M	H	L	L	M	L	L	M	M	L	L	L	M	M	H
CO4	M	H	L	L	M	L	L	M	M	L	L	L	M	M	H
CO5	M	H	M	L	M	M	M	M	M	M	L	L	M	M	H

Note: L- Low Correlation M -Medium Correlation H -High Correlation

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.
Statement: This course enables the student to realize the concepts of Linux operating system

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation
This course plays a major role in industry to provide Intelligent solutions that can be used to make sustainable industrialization and foster innovation

ECE 6224	EMBEDDED SYSTEMS LABORATORY	L	T	P	C
SDG: 4,8,9		0	0	2	1

COURSE OBJECTIVES:

COB1: To identify the software tools used in design of embedded systems with ARM processors.

COB2: To develop programming skills in design of ARM based embedded systems

COB3: To discuss the interface of peripherals with ARM Processors.

COB4: To explain the importance of multitasking and scheduling in RTOS.

COB5: To design and construct an Embedded system.

PREREQUISITES : Embedded system , Operating system

PRACTICALS

List of Experiments:

1. I\O Programming with ARM Processors.
2. Design with ARM Processors: ADC, DAC.
3. Timer Programming with ARM Processors.
4. Serial port Programming with ARM Processors.
5. Interrupt Programming with ARM Processors.
6. Interfacing LCD with ARM Processors.
7. Stepper motor interfacing with ARM Processors.
8. Multitasking in Real time Operating system(RTOS).
9. Scheduling in Real time Operating system(RTOS).
10. Interfacing sensors and actuators with SoC.

P – 30 ; TOTAL HOURS –30

TEXT BOOKS:

1. Andrew N. Sloss, Donimic Symes, Chris Wright, “ARM System Developer’s Guide” , The Morgan Kaufmann Series, 2004.
2. Steave Furber, “ARM system - on - chip architecture”, Addison Wesley, 2000
3. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edition. Netherlands: Newnes, 2009.

REFERENCES:

1. Shibu.K.V, “Introduction to Embedded Systems”, Tata Mcgraw Hill,2009 .
2. Lyla B Das,” Embedded Systems-An Integrated Approach”, Pearson 2013

COURSE OUTCOMES:

On completion of program students will be able to

CO1: develop simple application programs through Keil µ vision.

CO2: explain the I/O ports and timers of ARM Microcontrollers

CO3: interpret the use of multitasking techniques in real time operating systems.

CO4: analyse scheduling in real time operating systems.

CO5: develop applications with SoC.

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CO2	M	L	M	M	M	M	M	L	L	L	L	M	L	L	H
CO3	M	L	M	M	M	M	M	L	L	L	L	M	L	L	H
CO4	L	L	M	M	M	M	M	L	L	L	L	M	L	L	H
CO5	L	H	M	H	H	H	M	H	H	H	H	M	L	L	H

Note: L- Low Correlation M -Medium Correlation H -High Correlation

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement: Understanding of the Embedded Lab course will bring a global impact on quality education.

SDG 8: Development of new technologies provides sustainable economic growth and productive employment.

Statement: Design of new technologies based on Embedded System promotes sustained economic growth.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation

Statement: Able to apply the design concepts of Embedded systems to promote industrialization.

PROFESSIONAL ELECTIVES - VLSI DESIGN

ECEY 051	CAD FOR VLSI CIRCUITS	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To apply the fundamentals of CAD tools for the modelling, design, analysis, test, and verification of digital VLSI systems

COB2: To classify various layout design methods in VLSI

COB3: To define different partitioning algorithms in VLSI design

COB4: To identify the concepts behind the floor planning techniques

COB5: To select routing methods and learn about the hardware models for higher level synthesis

PREREQUISITES: Fabrication process of MOSFET

MODULE I VLSI DESIGN FLOW **9**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity- Tractable and Intractable problems - General purpose methods for combinatorial optimization.

MODULE II LAYOUT AND PARTITIONING **9**

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - Partitioning Algorithms - Group Migration Algorithm, Simulated Annealing and Evolution, Other Partitioning Algorithms - Performance Driven Partitioning.

MODULE III PLACEMENT **9**

Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement, Over-the-Cell Routing, Via Minimisation, Clock Routing, Power and Ground Routing.

MODULE IV FLOOR PLANNING AND ROUTING **9**

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

MODULE V HIGH LEVEL SYNTHESIS 9

Study of Hardware models for high level synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem.

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley & Sons, 2002.
2. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Springer International Edition, 2013.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed, 2011.

REFERENCES:

1. Erik Brunvand, “Digital VLSI Chip Design with Cadence and Synopsys CAD Tools”, Pearson, 2010.
2. Samir Palnitkar, “Verilog HDL”, Second Edition, Pearson Education, 2004.

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COURSE OUTCOMES:

On completion of program students will be able to

CO1: demonstrate the knowledge of CAD tools for the design of digital VLSI circuits

CO2:outline the physical layout design rules

CO3: discuss optimization algorithms in placement and partitioning.

CO4: illustrate the Floor planning concepts and its representation.

CO5: compare the various optimization algorithms in VLSI Routing

Board of Studies (BoS) :

23rd BOS of ECE held on 13.07.2022

Academic Council:

19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO 5	PO 6	PO7	PO8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	PSO 4
CO1	H	H	H	H	H	L	L	L	M	M	M	M	H	H	H	M
CO2	H	H	H	H	H	L	L	L	M	M	M	M	H	H	H	M
CO3	H	H	H	H	H	L	L	L	M	M	M	M	H	H	H	M
CO4	H	H	H	H	H	L	L	L	M	M	M	M	H	H	H	M
CO5	H	H	H	H	H	L	L	L	M	M	M	M	H	H	H	M

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4: Quality Education.
Statement: It is a elective course that explains the VLSI CAD flow which intend to provide quality education.

SDG 9: Industry, Innovation and Infrastructure
Statement: This course will deliver the concepts to fundamental design flow and algorithms for VLSI circuits which will enhance quality of life and to meet industry requirements.

ECEY 052	ASIC DESIGN	L	T	P	C
SDG: 4		3	0	0	3

COURSE OBJECTIVES:

COB1: To show the design flow of different types of ASIC

COB2: To Classify types of programming technologies and logic devices

COB3: To Compare various programmable ASIC architecture

COB4: To summarize System on Chip architecture

COB5: To analyze power reduction techniques and on-chip communication architecture of SoC

PREREQUISITES : VLSI Design Flow, IC layout

MODULE I ASIC DESIGN FLOW AND PROGRAMMABLE ASIC 9

Types of ASICs – Full custom ASIC- Standard cell based ASIC- Gate array based ASIC- Programmable logic devices architecture - ASIC Design flow - CMOS transistors, CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell.

MODULE II PROGRAMMABLE ASICs AND LOGIC CELLS 9

Antifuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

MODULE III ASIC PHYSICAL DESIGN 9

System partition -partitioning – partitioning methods – interconnect delay models and measurement of delay – floor planning – placement – Routing: global routing – detailed routing – special routing – circuit extraction – DRC.

MODULE IV INTRODUCTION TO SOC 9

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, On-Chip Communication Architecture Standards, Low-Power SoC Design

MODULE V SYNTHESIS OF ON-CHIP COMMUNICATION ARCHITECTURES AND TECHNIQUES FOR POWER REDUCTION 9

Bus Topology Synthesis- Hierarchical Bus Architecture Topology Synthesis -Bus Matrix (or Crossbar) Topology Synthesis-Component Mapping and Protocol Parameter Synthesis-Arbitration Scheme Synthesis -Bus Protocol Parameter Synthesis-Component Mapping and Protocol Parameter Synthesis-Techniques for Power Reduction-Schemes for Reducing Self-Switching Power-Schemes for Reducing Coupling Power

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. M.J.S. Smith, “Application Specific Integrated Circuits”, Pearson, 2003

REFERENCES:

1. H.Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1999.
2. J..M.Rabaey, A. Chandrakasan, and B.Nikolic, ”Digital Integrated Circuit Design Perspective (2/e)”, PHI 2003.
3. Hoi-Jun Yoo, Kangmin Leeand Jun Kyong Kim, “Low-Power NoC for High-Performance SoC Design”, CRC Press, 2008.
5. S.Pasricha and N.Dutt,” On-Chip Communication Architectures System on Chip Interconnect”, Elsveir, 2008.

COURSE OUTCOMES:

On completion of the course the student will be able to

CO1:explain VLSI tool-flow and FPGA architecture.

CO2:construct logic device using different programming technologies

CO3:illustrate the various programmable ASIC structure with its logic cells

CO4:to summarize the basics of System on Chip, On chip communication architectures like AMBA,AXI and utilizing Platform based design.

CO5: appreciate synthesis techniques and power reduction techniques.

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

Academic Council:
19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO1 1	PO 12	PSO1	PSO2	PSO3
CO1	L	M	M	M	M	M	M	M	M	M	M	M	H	L	L
CO2	L	M	M	M	M	M	M	M	M	M	M	M	H	L	L
CO3	L	M	M	M	M	M	M	M	M	M	M	M	H	L	L
CO4	L	M	M	M	M	M	M	M	M	M	M	M	H	L	L
CO5	L	M	M	M	M	M	M	M	M	M	M	M	H	L	L

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4: Quality Education.

Statement: It is a elective course that explains the VLSI CAD flow which intend to provide quality education.

ECEY 053	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C
SDG: 4,8,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To apply methods to design synchronous sequential circuits.

COB2: To apply different design approaches for asynchronous sequential circuits.

COB3: To summarize system design of ALU, UART and RISC processors.

COB4: To realize digital circuits using programmable logic devices.

COB5: Outline architectures of various programmable logic devices.

PREREQUISITES : Digital System design, FSM

MODULE I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN– State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits, Design of Arithmetic circuits for Fast adder- Array Multiplier.

MODULE II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Asynchronous sequential circuit design, Derivation of excitation table, Designing with SM charts – State machine charts, Derivation of SM charts, and Realization of SM charts-Hazards- Designing railway ticket vending Machine Controller.

MODULE III SYSTEM DESIGN 9

Design and Synthesis of Data-path Controllers – Partitioned sequential machines – – Design and synthesis of a RISC stored-program machine – Processor, ALU, Controller Design and Program Execution – UART – Operation, Transmitter, Receiver.

MODULE IV SYNCHRONOUS CIRCUIT DESIGN USING PROGRAMMABLE DEVICES 9

Programming Techniques -Re-Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects, Realize combinational, Arithmetic, Sequential Circuit with Programmable Array, Logic; Architecture and application of Field Programmable Logic Sequence.

MODULE V PROGRAMMABLE LOGIC DEVICES 9

Fold back Architecture with GAL, EPLD, EPLA , PEEL, PML; PROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill, 2017.
2. Parag K Lala, “Digital System design using PLD”, BS Publications, 2003.

REFERENCES:

1. Brian Holds worth, Clive Woods, “Digital Logic Design”, IV edition, Elsevier, 2008.
2. Charles H. Roth Jr., “Fundamentals of Logic design”, Thomson Learning, 2004.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1: design synchronous sequential circuit and iterative circuits.

CO2: model state machines, ASM charts and vending machine for the given design requirements.

CO3: designing digital systems such as ALU, UART and RISC processors.

CO4:use PLDs to design digital circuits.

CO5: model state machines using PLD & explain architectures of PLD.

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

Academic Council:
19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	L	M	M	M	M	M	M	M	H	H	H
CO2	H	H	H	H	L	M	M	M	M	M	M	M	H	H	H
CO3	H	H	H	H	L	M	M	M	M	M	M	M	H	H	H
CO4	H	H	H	H	L	M	M	M	M	M	M	M	H	H	H
CO5	H	H	H	H	L	M	M	M	M	M	M	M	H	H	H

Note : L- Low Correlation M -Medium Correlation H -High Correlation

SDG 4: Analysis and design of digital circuits promote Engineering skills and quality education.

SDG 8: Development of new technologies with digital circuits provides sustainable economic growth and productive employment.

SDG 9: Design of combinational and sequential circuits fosters innovation and sustainable industrialization.
Statement: Analysis, design and implementation of digital circuits promote sustained economic growth.

ECEY 054	NANO ELECTRONICS AND TECHNOLOGY	L	T	P	C
SDG: 9		3	0	0	3

COURSE OBJECTIVES:

COB1: To categorize nano-materials and the deposition Techniques.

COB2: To classify characterization of nano- materials.

COB3: To explain band structure models.

COB4: To select materials used for nano-electronics.

COB5: To show various electron transport mechanisms in nano structures.

PREREQUISITES : Fabrication in VLSI design, Atom and its Structures

MODULE I INTRODUCTION AND FABRICATION OF NANOMATERIALS **9**

Overview of nanotechnology, Historical background, Importance of Nanoscale, Bottom-up approaches, Top-down approaches, Functional approaches - Difference between bulk and nano materials - Size dependent properties - Fundamentals of film-Physical vapor deposition (PVD)-Chemical Vapor deposition (CVD)-Atomic layer deposition-sol gel films

MODULE II SYNTHESIS AND CHARACTERIZATION OF NANOMATERIALS **9**

Lithography - Assembly of nano-particles and nano-wires-other methods for micro fabrication - Structural characterization –X-ray diffraction, Small angle X-ray scattering, Scanning electron microscopy, Transmission electron microscopy, Scanning probe microscopy- Chemical characterization – Optical spectroscopy, Electron spectroscopy, Ion spectroscopy-Physical properties of nano-materials.

MODULE III FREE ELECTRON THEORY & THE NEW OHM'S LAW **9**

Electron flow, Classical free electron theory, Sommerfeld's theory, The quantum of conductance, Coulomb blockade, Towards Ohm's law. The Elastic Resistor: Conductance of an Elastic Resistor, Elastic Resistor- Heat dissipation.

MODULE IV MATERIALS FOR NANOELECTRONICS **9**

Semiconductors, Crystal lattices: bonding in crystals, Electron energy bands, Semiconductor hetero structures, Lattice-matched and pseudo morphic hetero structures, Inorganic nano-wires, Organic semiconductors, Carbon nano materials: nano- tubes and fullerenes.

MODULE V ELECTRON TRANSPORT IN SEMICONDUCTORS AND NANOSTRUCTURES **9**

Time and length scales of the electrons in solids, Statistics of the electrons in solids and nanostructures, Fermi statistics for electrons, the density of states of electrons in nanostructures, Electron transport in nanostructures.

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. Guozhong Cao, Ying Wang, “Nanostructures and Nano materials” world scientific series in nanoscience and nanotechnology 2nd edition 2016
2. Guozhong Cao, “Nanostructures and Nano Materials-Synthesis, Properties and Applications”, Imperial College Press, 2011.
3. M.S. Ramachandra Rao, Shubra Singh H, “Nano science and Nanotechnology: Fundamentals to Frontiers”, Wiley, 2013.
4. Charles P. Poole, Jr., Frank J. Owens, Introduction To Nanotechnology, John Wiley & Sons, Inc, 2003.

REFERENCES:

1. C.Dupas, P.Houdy, M.Lahmani, “Nanoscience: Nanotechnologies and Nanophysics”, Springer-Verlag Berlin Heidelberg, 2007.
2. Mick Wilson, Kamali Kannangara, Michells Simmons and Burkhard Raguse, “Nano Technology – Basic Science and Emerging Technologies”, 1st Edition, Overseas Press, New Delhi, 2005

COURSE OUTCOMES:

The students should be able to

CO1: infer the approaches used for fabricating the nano-materials.

CO2: apply the concept in synthesizing and characterizing nanomaterial.

CO3: define the electron theory and ohm’s law.

CO4: analyze the types of materials and the bonding.

CO5: compare the scaling of transistors and devices to smaller structures.

Board of Studies (BoS) : 23rd BOS of ECE held on 13.07.2022

Academic Council: 19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	H	M	M	H	H	H	H	H	H	H	M
CO2	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H
CO3	H	H	M	M	H	M	L	H	H	M	H	H	L	H	H
CO4	H	H	H	H	H	M	M	H	H	H	H	H	H	M	M
CO5	H	H	H	H	H	M	M	H	H	H	H	H	H	H	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 9 : Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation.

Statement :
The study on nanomaterial, its deposition techniques helps in deep understanding of the nano electronics.

ECEY 055	CMOS MIXED SIGNAL CIRCUIT DESIGN	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To discuss the phase locked loop and applications.

COB2: To analyze the digital to analog converting circuits and its specifications.

COB3: To model filter design using mixed-signal.

COB4: To develop and study the process of data conversion.

COB5: To Investigate switched capacitor circuits

PREREQUISITES :

- Electronic circuits, VLSI design, Analog integrated circuit design

MODULE I DATA CONVERTER 9

Sampling and Aliasing, The sample and Hold Impulse sampling, Data converter SNR - Quantization noise, Quantization noise, SNR – Improving SNR using averaging- Data Converter Design Basics - The One-Bit ADC and DAC - Passive Noise-Shaping- Improving SNR and Linearity- Improving Linearity Using an Active Circuit.

MODULE II NOISE SHAPING DATA CONVERTER 9

First order noise shaping – first order NS Modulators - RMS quantization noise in a first order modulator - Decimating and filtering the output of NS modulator - Analog implementation of first order NS modulator-Second order noise shaping - Noise shaping topologies - Higher order modulator - Multi bit modulator - Cascaded modulator – Band-pass modulators.

MODULE III BAND PASS DATA CONVERTER & HIGH-SPEED DATA CONVERTER 9

Continuous time band pass noise shaping-switched capacitor bandpass noise shaping - high speed converter topologies-Clocked signals –implementation and filtering-Generating clock signals in implementation.

MODULE IV PHASE LOCKED LOOP 9

Basic Phase-Locked Loop Architecture- Linearized Small-Signal Analysis- Jitter and Phase Noise- Electronic Oscillators- Jitter and Phase Noise in PLLS.

MODULE V FILTERS 9

Low Pass filters active RC integrators, MOSFET-C integrators, transconductance-C integrator, discrete time integrators. Filtering topologies - bilinear transfer function and bi-quadratic transfer function. Integrator-Based CMOS Filters: Integrator building blocks, filtering topologies, Filters using Noise-shaping.

L – 45 ; TOTAL HOURS – 45

REFERENCES:

1. Jacob Baker, “CMOS Mixed-Signal circuit design”, IEEE Press, 2009.
2. Razavi, “Design of analog CMOS integrated circuits”, McGraw Hill, 2017.
3. Razavi, “Principles of data conversion system design”, S.Chand and Company Ltd, 2011.
4. Jacob Baker, “CMOS: Circuit Design, Layout and Simulation”, IEEE Press, 2009.
5. Gregorian, Temes, “Analog MOS Integrated Circuit for signal processing”, John Wiley & Sons, 2008.
6. Allen, “CMOS Analog Circuit Design”, Oxford University Press, 3rd edition 2013.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1: design and analyze comparators, sample and hold circuits.

CO2: develop various noise shaping circuits for data converters.

CO3: analyze band pass and high-speed data converters.

CO4: implement various filters for mixed-signal circuits.

CO5: estimate the basic PLL circuits.

Board of Studies (BoS) : 23rd BOS of ECE held on 13.07.2022

Academic Council: 19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PO 12	PSO1	PSO2	PSO3	PSO 4
CO1	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H	M
CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H	M
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H	M
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H	M
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H	M

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4: Quality Education.

Statement: It is a core course that explains the various CMOS mixed circuit design which intends to provide quality education.

SDG 9: Industry, Innovation and Infrastructure

Statement: This course will deliver the concepts to design and innovate

Mixed circuits for modern electronic devices which will enhance the quality of life and to meet industry requirements.

ECEY 056	SYSTEM VERILOG PROGRAMMING	L	T	P	C
SDG: 4,9		2	0	0	2

COURSE OBJECTIVES:

COB1: To apply System Verilog concepts for verification.

COB2: Construct System Verilog and SVA for verification, and understand the improvements.

COB3: Outline use of classes, randomization, checking, and coverage

COB4: Demonstrate the concepts of assertions in system verilog.

PREREQUISITES : Verilog HDL, Digital VLSI Testing

MODULE I VERIFICATION GUIDELINES 7

Introduction, Verification Process, Verification Plan, Verification Methodology Manual, Basic Test bench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Test bench Components, Layered Test bench.

MODULE II DATA TYPES 8

Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types with type def, Creating User-Defined Structures, Enumerated Types, Constants, Strings.

MODULE III PROCEDURAL STATEMENTS AND ROUTINES 7

Procedural Statements, Tasks, Functions, and Void Functions.

MODULE IV SYSTEM VERILOG ASSERTIONS 8

Types of Assertions and examples Threads and Inter-process Communication: Working with Threads, Inter-process Communication, Events, Semaphores, Mailboxes, Building a Test bench with Threads and IPC.

L – 30; TOTAL HOURS – 30

TEXT BOOKS:

1. Chris Spear, System Verilog for Verification: A Guide to Learning the Test bench Language Features, Springer 2006.
2. Janick Bergeron, Writing Test benches Using System Verilog, Springer, 2006.
3. Tuart Sutherland, Simon David man and Peter Flake, System Verilog for Design: A Guide to Using System Verilog for Hardware Design and Modeling, 2nd Edition, Springer

REFERENCES:

1. Janick Bergeron ,Writing Test benches: Functional Verification of HDL Models, Second edition, , Kluwer Academic Publishers, 2003.
2. Mark Glasser ,Open Verification Methodology Cookbook, Springer, 2009
3. Andreas S. Meyer ,Principles of Functional Verification, , Elsevier Science, 2004
4. Harry D. Foster, Adam C. Krolnik, David J. Lacey, Assertion-Based Design, 2nd Edition, Kluwer Academic Publishers, 2004.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1: identify new constructs in System Verilog for verification

CO2: apply System Verilog to create re-usable models for digital designs

CO3: develop System Verilog to create test benches for digital designs

CO4: categorize system Verilog assertions for verification.

Board of Studies (BoS) : 23rd BOS of ECE held on 13.07.2022

Academic Council: 19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	PSO 4
CO1	H	H	H	H	H	L	L	M	M	M	M	M	H	H	H	H
CO2	H	H	H	H	H	L	L	M	M	M	M	M	H	H	H	H
CO3	H	H	H	H	H	L	L	M	M	M	M	M	H	H	H	H
CO4	H	H	H	H	H	L	L	M	M	M	M	M	H	H	H	H
CO5	H	H	H	H	H	L	L	M	M	M	M	M	H	H	H	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4: Quality Education

Statement :

This course will deliver the concepts of system Verilog for verification

SDG 9 : Industry, Innovation & Infrastructure

Statement :

System Verilog for verification enhance the students proficiency to battle the industry level standards.

ECEY 057	SCRIPTING LANGUAGES FOR VLSI DESIGN AUTOMATION	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To identify various verification techniques

COB2: To develop pearl scripts for automation.

COB3: To apply TCL scripts for automation.

COB4: To experiment with file management and process management using TCL and Pearl

COB5: To model UVM test bench environment

PREREQUISITES : Verification and testing methodologies, Linux basics

MODULE I PERL BASICS 9

History and Concepts of PERL - Scalar Data - Arrays and List Data - Control structures – Hashes - Basics I/O - Regular Expressions – Functions - Miscellaneous control structures - Formats.

MODULE II ADVANCED TOPICS IN PERL 9

Directory access - File and Directory manipulation - Process Management - Packages and Modules.

MODULE III TCL BASICS 9

An Overview of TCL and Tk -Tcl Language syntax – Variables – Expressions – Lists - Control flow – procedures - Errors and exceptions - String manipulations.

MODULE IV ADVANCED TOPICS IN TCL 9

Accessing files- Processes. Applications - Controlling Tools - Basics of Tk.

MODULE V UNIVERSAL VERIFICATION METHODOLOGY 9

Introduction to UVM - Verification components - Transaction level modelling - Developing

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. Larry Wall, Tom Christiansen, John Orwant, “Programming PERL”, Oreilly Publications, Fourth Edition, 2012.
2. John K. Ousterhout, Ken Jones, “Tcl and the Tk Toolkit”, Pearson Education, Second Edition, 2010.

3. Ray Salmei, “The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology” Boston Light Press; First edition, 2013.

REFERENCES:

1. Vanessa R. Copper, “Getting started with UVM: A Beginner’s Guide”, Verilab Publishing, First Edition, 2013.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1:analyze the verification methodology of VLSI circuits

CO2:compare scripts for VLSI design automation.

CO3:model pearl scripts for identification of sequential and combinational circuits.

CO4:classify TCL script to automate simulation process

CO5:infer UVM test bench for verification of VLSI circuits

Board of Studies (BoS) : 23rd BOS of ECE held on 13.07.2022

Academic Council: 19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4: Quality Education

Statement : This course will deliver the concepts of scripting language for verification

SDG 9 : Industry, Innovation & Infrastructure

Statement : To develop file management and process management in VLSI industry

ECEY 058	RF INTEGRATED CIRCUIT DESIGN	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To classify various impedance matching techniques

COB2: To build the methods of designing passive components in IC.

COB3: To explain concepts of amplifiers, oscillators and synthesizers.

COB4: To analyze the effect of noise in RF

COB5: To list the transceiver architectures.

PREREQUISITES : Basics of RF circuits, Amplifier circuits

MODULE I IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs. MOSFET amplifier controlled by AGC.

MODULE II FEEDBACK SYSTEMS AND POWER AMPLIFIERS 8

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, Power amplifiers- Switching Power Amplifiers, Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

MODULE III PLL AND FREQUENCY SYNTHESIZERS 8

Linearized Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer- N frequency synthesizers, Direct Digital Frequency synthesizers.

MODULE IV MIXERS AND OSCILLATORS 8

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators, Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

MODULE V NOISE AND TRANSCEIVER ARCHITECTURES 12

Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures up conversion Transmitter ,GSM radio architectures, CDMA, UMTS radio architectures.

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. Steer, Michael, “Microwave and RF design”, NC State University, 3e, 2019.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 2e, 2013.

REFERENCES:

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004, Reprint 2009.
2. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2e, 2017.
3. Voinigescu, Sorin, “High-frequency integrated circuits”, Cambridge University Press, 2013.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1: classify the impedance matching techniques.

CO2: analyze Low Noise and power amplifier circuits and design the same based on the given requirements

CO3: describe and analyze the performance of frequency synthesizers

CO4: analyze mixers and oscillator circuits and design the same based on the given requirements.

CO5: model the building blocks of RF transceiver system

Board of Studies (BoS) :

23rd BOS of ECE held on 13.07.2022

Academic Council:

19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	H	M	M	H	H	H	H	H	H	H	H
CO2	H	H	H	H	H	M	M	H	H	H	H	H	H	H	H
CO3	H	H	H	H	H	M	M	H	H	H	H	H	H	H	H
CO4	H	H	H	H	H	M	M	H	H	H	H	H	H	H	H
CO5	H	H	H	H	H	M	M	H	H	H	H	H	H	H	H

Note: L- Low Correlation M -Medium Correlation H -High Correlation

SDG 4: Quality Education
Statement: This course will deliver the RF technology in IC

SDG 9: Industry, Innovation & Infrastructure
Statement : To develop advanced noise cancellation techniques

ECEY 059	NETWORK ON CHIP	L	T	P	C
SDG: 4, 9		3	0	0	3

COURSE OBJECTIVES:

COB1: To explain basic concepts in the implementation of networks-on-chip (NoC) technology.

COB2: To Identify the NoC paradigm and its architecture design.

COB3: To compare low-power techniques for NoC technology.

COB4: To enhance the students skill on Signal Integrity of Network-on-Chip.

COB5: To examine development of application specific NoC.

PREREQUISITES : Circuits & Network Analysis

MODULE I NETWORK ON CHIP (NOC) BASICS AND INTERCONNECTION NETWORKS IN NETWORK-ON-CHIP **9**

Introduction to NoC, Evolution of NoC from SoC , Network Topologies , Switching Techniques, Routing Strategies, Flow Control Protocol, Quality-of-Service Support.

MODULE II ARCHITECTURE DESIGN OF NETWORK-ON-CHIP **10**

Switching Techniques and Packet Format, Asynchronous FIFO Design, GALS Style of Communication, Wormhole Router Architecture Design, VC Router Architecture Design, Adaptive Router Architecture Design.

MODULE III LOW-POWER TECHNIQUES FOR NETWORK-ON-CHIP **7**

Standard Low-Power Methods for NoC Routers, Standard Low-Power Methods for NoC Links, System-Level Power Reduction.

MODULE IV SIGNAL INTEGRITY AND RELIABILITY OF NETWORK-ON-CHIP **9**

Sources of Faults in NoC Fabric, Permanent Fault Controlling Techniques, Transient Fault Controlling Techniques, Unified Coding Framework, Energy and Reliability Trade-Off in Coding Technique.

MODULE V APPLICATION-SPECIFIC NETWORK-ON-CHIP SYNTHESIS (ASNOC) 10

ASNoC Synthesis Problem, System-Level Floor planning, Custom Interconnection Topology and Route Generation, ASNoC Synthesis with Flexible Router Placement

L – 45; TOTAL HOURS – 45

TEXT BOOKS:

1. Santanu Kundu, Santanu Chattopadhyay, “Network-on-Chip: The Next Generation of System on-Chip Integration”, CRC Press, 2017.
2. Fayez Gebali, Haytham Elmiligi, Mohamed Watheq El-Kharashi, Network son-Chips: Theory and Practice, CRC Press, 2017.

REFERENCES:

1. Sudeep Pasricha, NikilDutt, “On-Chip Communication Architectures: System on Chip Interconnect”, Morgan Kaufmann, 2010.
2. José Flich and Davide Bertozzi, “Designing Network On-Chip Architectures in the Nanoscale Era”, Chapman and Hall/CRC, 2011.
3. Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, “System-On-Chip Test Architectures: Nanometer Design For Testability”, Elsevier, 2008.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1: discuss the evolution of NoC from SoC.

CO2: identify the concepts of interconnection of networks in Network-on-Chip.

CO3: analyse the various architectural designs on NoC

CO4:choose appropriate low power techniques for power reduction applications.

CO5: apply the fault controlling techniques for reliable NoC and synthesis application specific NoC technology.

Board of Studies (BoS) :	**Academic Council:**
23rd BOS of ECE held on 13.07.2022	19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO1 1	PO 12	PSO1	PSO2	PSO3
CO1	H	H	M	L	L	L	L	L	L	L	L	L	H	L	H
CO2	M	H	H	M	L	L	L	L	L	L	L	L	H	L	H
CO3	M	H	H	M	L	L	L	L	L	L	L	L	H	L	H
CO4	L	M	H	H	M	L	L	L	L	L	L	L	H	L	H
CO5	L	L	L	M	H	L	L	L	L	L	L	L	H	L	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4: Quality Education

Statement: This course will deliver the concepts of Network on Chip technology.

SDG 9 : Industry, Innovation & Infrastructure

Statement: Network on chip architectural framework enhances the students skill to compete the industry level standards.

ECEY 060	SOC DESIGN AND VERIFICATION	L	T	P	C
SDG: 4, 9		3	0	0	3

COURSE OBJECTIVES:

COB1: To explain System on Chip and develop power optimization techniques.

COB2: Develop SoC designs in industrial environment using different design methodologies

COB3: Examine the on chip components interconnected in a SoC

COB4: Analyze and solve problems in traditional bus based communication architecture using network on chip.

COB5: Model SoC based processor design

PREREQUISITES: Digital Electronics, Analog Electronics

MODULE I INTRODUCTION TO SOC DESIGN 9

Basic overview of system on chip-Motivation for SoC Design –developments in SoC design and test methodologies. Review of Moore's law and CMOS scaling, benefits of system-on chip integration. Comparison on System-on-Board, System-on-Chip, and System-in-Package- SoC design challenges. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.

MODULE II SYSTEM ON CHIP DESIGN PROCESS & INTERCONNECTIONS 9

A canonical SoC Design, SoC Design flow waterfall vs spiral, top down vs Bottom up. Specification requirement, Types of Specification, System Design process, System level design issues, Soft IP Vs Hard IP, Design for timing closure, Logic design issues, Verification strategy, On Chip Buses. Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies.

MODULE III HARDWARE AND SOFTWARE DESIGN 9

Hardware-Software code sign, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc. Embedded Memories –cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence, MESI protocol and Directory-based coherence.

MODULE IV SoC VERIFICATION 9

Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co-verification and Static net list verification. Verification architecture, Verification components, Introduction to VMM, OVM and UVM.

MODULE V SoC with PROCESSORS 9

Introduction to ARM cortex M , Introduction to system design with cortex M processor, Building simple bus system for cortex M processor, Debug integration with cortex M processor system, Basic concepts in Processor Micro Architecture, VLIW Processors, Superscalar Processors .

L – 45; TOTAL HOURS –45

TEXT BOOKS:

1. Prakash Rashinkar, Peter Paterson and Leena Singh, “SoC Verification Methodology and Techniques”, Kluwer Academic Publishers, 2002.
2. Michael Keating, Pierre Bricaud, “Reuse Methodology manual for System on A Chip Designs”, Kluwer Academic Publishers, second edition, 2001.
3. William K. Lam, “Design Verification: Simulation and Formal Method based Approaches”, Prentice Hall, 2005.
4. Joseph Yiu, “System-on-Chip Design with Arm® Cortex® -M Processors”, ARM Education Media, 2019.

REFERENCES:

1. Rochit Rajsuman, “System- on -a- Chip Design and Test”, ISBN, 2000.
2. A.A. Jerraya, W.Wolf “Multiprocessor Systems on chips”, M K Publishers, 2004.
3. Laung-Terng Wang, Charles Stroud, Nur Touba, “System-on-Chip Test Architectures” 1st Edition, Elsivier, 2007.
4. Dirk Jansen “The EDA Hand Book”, Kluwer Academic Publishers, 2010.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1: analyze CMOS VLSI Technologies along with performance parameters
CO2: describe the top-down, bottom-up design flows and discuss timing problems.
CO3: construct data path elements such as ALUs, Multipliers.

CO4: compare various power optimization and timing issues related to complex digital systems

CO5: explain the bus architectures of NOCs and routing.

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

Academic Council:
19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	H	M	M	H	H	H	H	H	H	H	H
CO2	H	H	H	H	H	L	M	H	H	H	H	H	H	H	H
CO3	H	H	M	M	H	M	M	H	H	M	H	H	L	H	H
CO4	H	H	H	H	H	M	M	H	H	H	H	H	H	M	M
CO5	H	H	H	H	H	M	M	H	H	H	H	H	H	H	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4: Quality Education
Statement : This course will deliver the concepts of Network on Chip technology.

SDG 9 : Industry, Innovation & Infrastructure, Statement :
Network on chip architectural framework enhances the students skill to compete the industry level standards.

ECEY 061	TESTING OF VLSI CIRCUITS	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: Extend automated and manual techniques for generating tests for faults in digital circuits and systems.

COB2: Show generation of test vectors for combinational and sequential circuits

COB3: Develop built in self test patterns.

COB4: Classify Crosstalk faults effects and test pattern generation .

COB5: Classify Testing of algorithms for digital circuits.

PREREQUISITES : VLSI Design, Fault models

MODULE I INTRODUCTION TO VLSI TESTING AND FAULT MODELLING 9

Introduction to VLSI testing- Importance of testing, Challenges in VLSI testing, Levels of abstractions in VLSI testing. Fault Types, Functional Vs Structural Testing, Levels of Fault Models, Fault Equivalence, Equivalence of Single Stuck-at Faults, Fault Collapsing, Fault Dominance. Logic & Fault Simulation- Simulation for Design Verification , Simulation for Test Evaluation Modeling Circuits for Simulation, Algorithms for True-Value Simulation &Fault Simulation. SCOAP –Combinational complexity and observability.

MODULE II COMBINATIONAL AND SEQUENTIAL TEST GENERATION 9

Combinational Circuit Test Generation-Algorithms and Representations, Structural vs. Functional Test, Automatic Test-Pattern Generator, Search Space Abstractions ,Algorithm Completeness, ATPG Algebras, Algorithm Types, Redundancy Identification (RID), Significant Combinational ATPG Algorithms- D-Calculus and D-Algorithm (Roth) , PODEM . Sequential Circuit Test Generation- ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, Cycle-Free Circuits, Cyclic Circuits.

MODULE III MEMORY TESTING AND DESIGN FOR TESTABILITY 9

RAM Functional Fault Models and Test Algorithms, RAM Fault Simulation and Test Algorithm Generation, Memory Built-In Self-Test, Design for Testability Basics -Ad Hoc Approach, Structured Approach .Scan Cell Designs - Scan

Architectures, Full-Scan Design, Muxed-D Full-Scan Design , Clocked Full-Scan Design , LSSD, Partial-Scan Design , Scan Design Rules , Scan Design Flow, Special-Purpose Scan Designs, RTL Design for Testability.

MODULE IV BUILT-IN SELF-TEST 9

Built-in Self-Test Design rules -Test Pattern Generation for BIST-Exhaustive Testing –Exhaustive testing-Pseudo-random testing- Delay fault Testing - Output Response Analysis -Transition Count- Signature Analysis -BIST Architectures -Built-in Logic Block Observer- Modified Built-in Logic Block Observer -circular self test path.

MODULE V BOUNDARY SCAN AND CORE-BASED TESTING 9

Digital boundary scan-Boundary scans for advanced networks- Embedded core test standard-analog and mixed signal testing. FPGA Testing, MEMS Testing, RF Testing.

L- 45 ; TOTAL HOURS –45

TEXT BOOKS:

1. Parag K. Lala, “An Introduction to Logic Circuit Testing”, Texas A&M University–Texarkana, 2009.
2. Angela kristic, “Delay fault testing for VLSI circuits”, Springer science, 2013.
3. S.Jayanthy, MC Bhuvaneshwari, “Test generation of cross talk delay faults in VLSI circuits”, Springer, 2019.

REFERENCES:

1. Bushnell and Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits”, Kluwer Academic Publishers, 2002
2. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
3. Laung-Terng Wang , Cheng-Wen Wu , Xiaoqing Wen , Khader and S. Abdel-Hafez ,”VLSI Test Principles and Architectures: Design for Testability”, Morgan Kaufmann; 1st edition, 2006.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1:genarate test vectors using stuck at models for combinational circuits

CO2:model circuit with testability perspective

CO3:generate test vector for sequential circuits

CO4: show the architecture of built in self test and fault diagnosis.
CO5: design the test pattern for cross talk fault.

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

Academic Council:
19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO1 1	PO 12	PSO1	PSO2	PSO3
CO1	H	H	H	H	H	M	M	H	H	H	H	H	H	H	M
CO2	H	H	H	H	H	M	M	H	H	H	H	H	H	H	H
CO3	H	H	M	M	H	M	M	H	H	M	H	H	H	H	H
CO4	H	H	H	H	H	M	H	H	H	H	H	H	H	M	M
CO5	H	H	H	H	H	M	M	H	H	H	H	H	H	H	H

SDG 4: Quality Education
Statement : This course will deliver the concepts of Testing and verification in VLSI design

SDG 9 : Industry, Innovation & Infrastructure, Statement :
Fault model techniques enhances the process of fault coverage in VLSI circuits

ECEY 062 VLSI DIGITAL SIGNAL PROCESSING L T P C

SDG: 3, 9 3 0 0 3

COURSE OBJECTIVES:

COB1: Explain the fundamentals of VLSI signal processing.

COB2: Build and optimize VLSI architectures for basic DSP algorithms

COB3: Interpret the VLSI design models in various domains of signal processing

COB4: Model the signal processing architectures for arithmetic operations

COB5: Develop applications of parallel processing and pipelining

PREREQUISITES : DSP, Computer Architecture

MODULE I PIPELINING AND PARALLEL PROCESSING 10

Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

MODULE II UNFOLDING 7

Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding.

MODULE III FOLDING 8

Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.

MODULE IV SYSTOLIC ARCHITECTURE DESIGN 10

Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

MODULE V FAST CONVOLUTION 10

Introduction, Cook, Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

L – 45; TOTAL HOURS –45

TEXT BOOKS:

1. Pramod Kumar Meher, “Arithmetic Circuits for DSP Applications”, Wiley IEEE press, 2017.
2. Hongjiang Song, ”Principles of VLSI Design - Symmetry, Structures and Methods”, Lulu Publishers, 2018.

REFERENCES:

1.Keshap K. Parhi, VLSI Digital Signal Processing Systems, Design and Implementation, John Wiley, 2007.

2.U. Meyer – Baese, “Digital Signal Processing with Field Programmable Gate Arrays”, Springer, Second Edition, 2004.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1: categorize various algorithms that can be designed and applied on application specific VLSI architecture

CO2: develop fast convolution algorithms and high speed multipliers to improve the efficiency of DSP processors

CO3: select basic architectures for DSP using CAD tools.

CO4:develop FIR digital filters using parallel processing.

CO5: model Cook Toom Algorithm, Winogard Algorithms for fast convolution.

Board of Studies (BoS) : 23rd BOS of ECE held on 13.07.2022

Academic Council: 19th Academic Council held on 29.09.2022

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PO 12	PSO1	PSO2	PSO3
CO1	H	H	M	L		M	M	M	M	M			L	H	L
CO2	M	H	H	M	L	M	M	M	M	M				H	
CO3	M	H	H	M	L	M	M	M	M	M			L	H	
CO4		M	H	H	M	M	M	M	M	M				H	
CO5				M	H	M	M	M	M	M			L	H	

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 3 : Good Health and Well-Being

Statement : Signal processing plays a major role in medical instrumentation. A sound knowledge in these could lead to a substantial research and development in health and well-being.

SDG 9 : Industry, Innovation & Infrastructure

Statement : Signals and its processing forms the basis of control systems and automation.

ELECTIVE COURSES - EMBEDDED SYSTEM

ECEY 024	**INTERNET OF THINGS**	**L**	**T**	**P**	**C**
SDG: 4,9		**3**	**0**	**0**	**3**

COURSE OBJECTIVES:

COB1: To explain IoT Architecture and Technology

COB2: To classify IoT protocols

COB3: To Compare different IoT Hardware platforms

COB4: To inspect application development for mobile Platforms

COB5: To make use of appropriate IoT solutions and recommendations according to the applications used.

PREREQUISITES:

Computer Networks, Embedded Systems

MODULE I INTRODUCTION 9

IoT- Architectural Overview – Design principles - IoT Technology Fundamentals- Devices and gateways, Local and wide area networking, Data management, Business processes in IoT- Interoperability - Types of Interoperability Connectivity, Interoperability at Present state - Key Challenges- Introduction to Web Servers and Cloud Computing - Basics of Big Data and Data Science.

MODULE II IoT ARCHITECTURE AND APPLICATIONS 9

Architecture: M2M – Machine to Machine, Web of Things, IoT protocol, Introduction to wireless and mobile networks, ZigBee, BLE mesh, WiFi, LoRa, Applications: remote monitoring & sensing, remote controlling, performance analysis.

MODULE III IoT PLATFORM OVERVIEW 9

Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards. Network Fundamentals: Overview and working principle of Wired Networking equipment – Router, Switches, Overview and working principle of Wireless Networking equipment, Linux Network configuration Concepts.

MODULE IV IoT APPLICATION DEVELOPMENT 9

Application Protocols-MQTT, REST/HTTP, CoAP, MySQL -Back-end Application -Design Apache for handling HTTP Requests, PHP & MySQL for data processing, MongoDB Object type Database, HTML, CSS & jQuery for UI Designing, JSON lib for data processing, Security & Privacy during development, Application Development for mobile Platforms: Overview of Android App Development tools.

MODULE V CASE STUDY & ADVANCED IoT APPLICATIONS 9

IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipment. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards.

L – 45; TOTAL HOURS –45

TEXT BOOKS:

1. Jean-Philippe Vasseur, Adam Dunkels, “Interconnecting Smart Objects with IP: The Next Internet”, Morgan Kuffmann-2010
2. Vijay Madisetti , Arshdeep Bahga, : Internet of Things (A Hands-on-Approach)” -2014
3. Adrian McEwen (Author), Hakim Cassimally, “Designing the Internet of Things” ,Wiley -2013
4. Dr. Ovidiu Vermesan, Dr. Peter Friess, “Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems,” River Publishers -2013.

REFERENCES:

1. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, “From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence”, 1st Edition, Academic Press, 2014.
2. Barrie Sosinsky, “Cloud Computing Bible”, Wiley-India, 2010
3. Asoke K Talukder and Roopa R Yavagal, “Mobile Computing,” Tata McGraw Hill, 2010.
4. Adelstein and S.K.S. Gupta, “Fundamentals of Mobile and Pervasive Computing”, McGraw Hill, 2009.
5. Ronald L. Krutz, Russell Dean Vines, “Cloud Security: A Comprehensive Guide to Secure Cloud Computing”, Wiley-India, 2010.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1:identify the key technologies of IoT and cloud computing.

CO2: relate the architecture and infrastructure of IoT.

CO3: interpret the core issues of IoT such as security, privacy, and interoperability.

CO4: choose the appropriate technologies, algorithms, and approaches for IoT.

CO5: create new ideas and innovations in IoT applications.

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

Academic Council:
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CO1	H	H	H	H	L	L	L	M	M	H	H	H	H	H	H
CO2	H	H	H	H	L	L	L	M	M	H	H	H	H	H	H
CO3	H	H	H	H	L	L	L	M	M	H	H	H	H	H	H
CO4	H	H	H	H	L	L	L	M	M	H	H	H	H	H	H
CO5	H	H	H	H	L	L	L	M	M	H	H	H	H	H	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4: Quality Education

Statement : The architecture and applications of IoT are explored in real time systems

SDG 9 : Industry, Innovation & Infrastructure

Statement : Industry standard protocols and platforms of IoT are stuidied

ECEY 025	INDUSTRY 4.0	L	T	P	C
SDG: 9		3	0	2	4

COURSE OBJECTIVES:

COB1: To explain concepts, main trends and the paradigm of Industry 4.0

COB2:To Analyze the IoT technologies for practical IoT applications

COB3: ToDevelop the ability to use Internet of Things related protocols and connectivity methods

COB4: To show design concepts of Industrial IOT Systems for various application.

COB5: To examine design and analysis of Industry 4.0

PREREQUISITES: Robotics, Cloud computing

MODULE I INTRODUCTION TO INDUSTRY 4.0 9+6

The Various Industrial Revolutions, Digitalisation and the Networked Economy, Drivers, Enablers, Compelling Forces and Challenges for Industry 4.0, The Journey so far: Developments in USA, Europe, China and other countries, Comparison of Industry 4.0 Factory and Today's Factory, Trends of Industrial Big Data and Predictive Analytics for Smart Business Transformation

Practical:1. Measure the light intensity in the room and output data to the web API.

MODULE II ROAD TO INDUSTRY 4.0& RELATED DISCIPLINES 9+6

Internet of Things (IoT) & Industrial Internet of Things (IIoT) & Internet of Services, Smart Manufacturing, Smart Devices and Products, Smart Logistics, Smart Cities, Predictive Analytics

Cyber physical Systems, Robotic Automation and Collaborative Robots, Support System for Industry 4.0, Support System for Industry 4.0, Cyber Security

Practical:1. Build a web based application to automate door that unlocks itself using facial recognition.

MODULE III DATA INFORMATION AND COLLABORATION 9+6

Resource-based view of a firm, Data as a new resource for organizations, Harnessing and sharing knowledge in organizations, Cloud Computing Basics, Cloud Computing and Industry 4.0

Practical:1. IoT based Healthcare application

MODULE IV BUSINESS ISSUES IN INDUSTRY 4.0 9+6

Opportunities and Challenges, Future of Works and Skills for Workers in the Industry 4.0 Era, Strategies for competing in an Industry 4.0 world

Practical:1. Real-time environmental monitoring and weather prediction

MODULE V INDUSTRY 4.0 APPLICATIONS 9+6

Industrial IoT- Application Domains: Healthcare, Power Plants, Inventory Management & Quality Control, Plant Safety and Security, Oil, chemical and pharmaceutical industry, Applications of UAVs in Industries, Real case studies.

Practical:1. Plant health monitoring

L –45 ; P-30; TOTAL HOURS –75

TEXT BOOKS:

1. Alp Ustundag and Emre Cevikcan, “Industry 4.0: Managing the Digital Transformation”, Springer, 2017.
2. Alasdair Gilchrist, "Industry 4.0: The Industrial Internet of Things" Apress, 2017.
3. Deepak Gupta, Victor Hugo C. de Albuquerque, Ashish Khanna, Purnima Lala Mehta "Smart Sensors for Industrial Internet of Things: Challenges, Solutions and Applications", Springer, 1st Edition, 2021.
4. Francis daCosta, “Rethinking the Internet of things: A Scalable Approach to Connecting Everything”, Apress, 2014.

REFERENCES:

1. Christoph Jan Bartodziej, "The Concept Industry 4.0: An Empirical Analysis of Technologies and Applications in Production Logistics", Springer, 2016
2. Gary Smart, "Practical Python Programming for IoT: Build advanced IoT projects using a Raspberry Pi 4, MQTT, RESTful APIs, Web Sockets, and Python 3" Pckt Publishing, 2020
3. Dr. Ovidiu Vermesan, Dr. Peter Friess, “Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems”, River Publishers, 2013.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1:categorize Knowledge of theory and practice related to Industrial IoT Systems

CO2:identify, formulate and solve engineering problems by using Industrial IoT

CO3:implement real field problems of Industrial applications with IoT capability

CO4:develop hands on experience with IoT techniques
CO5:develop a real time IoT system

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

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CO1	H	H	M	M	L	L	L	L	L	L	L	L	H	H	H
CO2	M	H	M	M	L	L	L	L	L	L	L	L	H	H	H
CO3	M	M	L	M	L	L	L	L	L	L	L	L	H	H	H
CO4	H	M	M	M	L	L	L	L	L	L	L	L	H	H	H
CO5	H	H	M	M	L	L	L	L	L	L	L	L	H	H	H

Note: L- Low Correlation M -Medium Correlation H -High Correlation

SDG 9 : Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation,

Able to apply the theoretical concepts for the various application Industry 4.0

ECEY 026	ARTIFICIAL INTELLIGENCE	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To discuss on artificial intelligence principles, techniques

COB2: To assess the applicability, strengths, and weaknesses of the basic knowledge representation, problem solving, and learning methods in solving engineering problems

COB3: To develop intelligent systems by assembling solutions to concrete computational problems

COB4: Evaluate Artificial Intelligence (AI) methods and describe their foundations

COB5:To determine appropriate Artificial Intelligence (AI) methods to solve various engineering problems

PREREQUISITES: Probability, linear algebra and data structures

MODULE I ARTIFICIAL INTELLIGENCE AND ITS ISSUES 6

Importance of AI, Evolution of AI - Applications of AI, Classification of AI systems, Knowledge Inferring systems and Planning, Uncertainty and Learning Systems.

MODULE II PROBLEM SOLVING TECHNIQUES 9

Problem solving by Search, Problem space - State space, Blind Search - Types, Performance measurement.

MODULE III HEURISTIC SEARCH AND KNOWLEDGE BASED SYSTEMS 10

Min-max algorithm, Alpha-Beta Pruning, Logical systems, Knowledge Based systems, Propositional Logic Constraints, Predicate Logic-First Order Logic, Ontological representations and applications.

MODULE IV UNCERTAINTY AND KNOWLEDGE REASONING 10

Overview of uncertainty, Bayes Rule Inference, Belief Network, Utility Based System, Decision Network.

MODULE V LEARNING SYSTEMS AND EXPERT SYSTEMS 10

Forms of Learning Types - Supervised, Unsupervised, Reinforcement Learning, Learning Decision Trees, Expert Systems - Stages in the development of an Expert System - Probability based Expert Systems - Expert System Tools - Difficulties in Developing Expert Systems – Applications of Expert Systems.

L –45 ; TOTAL HOURS –45

TEXT BOOKS:

1. Russell, S. and Norvig, P, “Artificial Intelligence - A Modern Approach”, 3rd edition, Prentice Hall, 2016.
2. Poole, D. and Mackworth, A, “Artificial Intelligence: Foundations of Computational Agents, Cambridge University Press, 2017.

REFERENCES:

1. Rich, E., Knight, K and Shankar, B. “Artificial Intelligence”, 3rd edition, Tata McGraw Hill, 2019.
2. Luger, G.F.,” Artificial Intelligence -Structures and Strategies for Complex Problem Solving” 6th edition, Pearson, 2008.
3. Brachman, R. and Levesque, H., “Knowledge Representation and Reasoning”, Morgan Kaufmann, 2004.
4. Alpaydin, E, “Introduction to Machine Learning. 2nd edition, MIT Press, 2014
5. Sutton R.S. and Barto, A.G.,”Reinforcement Learning: An Introduction”, MIT Press, 2018.
6. Padhy, N.P., “Artificial Intelligence and Intelligent Systems”, Oxford University Press, 2009.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1: evaluate Artificial Intelligence (AI) methods and describe their foundations

CO2: apply basic principles of AI in solutions that require problem solving, inference, perception, knowledge representation and learning

CO3: demonstrate knowledge of reasoning and knowledge representation for solving real world problems

CO4: analyze and illustrate how search algorithms play vital role in problem solving

CO5:explain the construction of learning and expert systems

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23rd BOS of ECE held on 13.07.2022	19th Academic Council held on 29.09.2022

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CO1	H	H	H	H	H	H	M	M	M	M	M	M	H	H	H
CO2	H	H	H	H	H	H	M	M	M	M	M	M	H	H	H
CO3	H	H	H	H	H	H	M	M	M	M	M	M	H	H	H
CO4	H	H	H	H	H	H	M	M	M	M	M	M	H	H	H
CO5	H	H	H	H	H	H	M	M	M	M	M	M	H	H	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG No: 4 -Quality Education

This course will deliver the basic concepts of neural networks which is mostly used in Artificial Intelligence.

SDG No: 9 - Industry, Innovation and Infrastructure

Artificial intelligence plays major roles in industry and modern infrastructures. Innovative ideas can be implemented by programming.

ECEY 027	MACHINE LEARNING FOR EMBEDDED SYSTEMS	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To impart knowledge on regression and classification models

COB2: To gain knowledge of clustering and dimensionality reduction techniques

COB3: To know machine learning embedded hardware and software

COB4: To discuss the performance of embedded system machine learning

COB5: To apply the machine learning techniques in applications.

PREREQUISITES: Linear Algebra and Data structure

MODULE I SUPERVISED LEARNING ALGORITHMS 5

Introduction to AI, Machine Learning(ML) techniques, Regression -Linear regression, Gradient Descent, Multiple Linear Regression, Evaluation Measures of models, Bias and variance tradeoff -Classification- Logistic Regression, Support vector machines, K Nearest Neighbours, Decision Tree.

MODULE II UNSUPERVISED LEARNING ALGORITHMS 9

Introduction, K-Means clustering Algorithm, Hierarchical clustering- Dimensionality Reduction -Factor analysis-Principal components analysis-Independent components analysis- Recommender system, Artificial neural network

MODULE III MACHINE LEARNING ON EMBEDDED DEVICES 9

Machine Learning Specific Hardware and Software- Machine Learning on Microcontrollers- Getting Started with Edge Impulse- Data Collection- Feature Extraction from Motion Data- Feature Selection in Edge Impulse- Machine Learning Pipeline

MODULE IV ML MODEL EVALUATION AND DEPLOYMENT 11

Model Training in Edge Impulse- Underfitting and Overfitting- Use a Model for Inference- Testing Inference with a Smartphone- Deploying a Trained Model to embedded board -Anomaly Detection

MODULE V CASE STUDY 11

Motion Detection-Audio classification and Keyword Spotting- Introduction to Audio Classification- Audio Data Capture- Audio Feature Extraction- Convolutional Neural Networks- Deploy Keyword Spotting System- Implementation Strategies-Sensor

Fusion.

L – 45 ; TOTAL HOURS – 45

REFERENCES:

1. Ethemlpaydin, ”Introduction to Machine Learning”, MIT Press, Prentice Hall of India, Third Edition, 2014.
2. Ian H. Witten, Eibe Frank, Mark A. Hall, “Data Mining: Practical Machine Learning Tools and Techniques”, 3rd Edition, Morgan Kaufmann, 2011.
3. Thinking machines- SHIGEYUKI0 , Academic Press, 2021.

COURSE OUTCOMES:

At the end of the course, the student should be able to:

CO1: Discuss the fundamental concepts of a machine learning

CO2: Identify suitable mathematical technique for machine learning problems

CO3: Develop a machine learning model using the latest embedded system boards.

CO4: Apply the methods to improve the performance of the embedded systems

CO5: Solve the problems using machine learning methods.

Board of Studies (BoS): 23rd BOS of ECE held on 13.07.2022

Academic Council: 19th Academic Council held on 29.09.2022

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CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG No: 4 -Quality Education

This course will deliver the basic concepts of neural networks which is mostly used in Artificial Intelligence machine systems.

ECEY 077	REAL TIME SYSTEMS	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To define the fundamental concepts of real time systems

COB2: To outline the various Uniprocessor and Multiprocessor scheduling mechanisms

COB3: To develop knowledge on programming languages and tools for real time systems.

COB4: To elaborate overview of real time data bases

COB5: To Classify the Fault Tolerance and evaluation techniques in real time systems.

PREREQUISITES: Embedded Systems, Operating Systems

MODULE I INTRODUCTION TO REAL TIME SYSTEM 9

Introduction –characterizing real time system -Performance Measures for Real Time Systems – Estimating Program Run Times – Task Assignment and Scheduling.

MODULE II PROGRAMMING LANGUAGES AND TOOLS 9

Desired language characteristics – ADA language - Data typing – Control structures – Facilitating Hierarchical Decomposition- Packages- Run time Error handling – Overloading and Generics – Multitasking – Timing Specifications – Programming Environments – Run time support.

MODULE III REAL TIME DATABASES 9

Basic Definition, Real time Vs General Purpose Databases- Main Memory Databases- Transaction priorities-Transaction Aborts-Concurrency control issues-Disk Scheduling Algorithms-Two – phase Approach to improve Predictability – Maintaining Serialization Consistency – Databases for Hard Real Time Systems.

MODULE IV REAL TIME COMMUNICATION 9

Communications media, Network Topologies, Protocols- contention based, Token based, Stop-and-Go multihop, Polled Bus, Hierarchical Round Robin Protocol, Deadline-Based Protocols, Fault Tolerant Routing.

MODULE V FAULT TOLERANT AND EVALUATION TECHNIQUES 9

Fault Tolerance Techniques – Fault Types – Fault Detection-Fault and Error containment- Redundancy- Reliability Evaluation Techniques – Software error models.

L –45 ; TOTAL HOURS –45

TEXT BOOKS:

1. C.M. Krishna, Kang G. Shin, “Real – Time Systems”, McGraw – Hill International Editions, 2010.
2. Rajib Mall, ”Real-time systems: theory and practice”, Pearson Education, 2007.
3. Peter D.Lawrence, “Real Time Micro Computer System Design – An Introduction”, McGraw Hill, 1988.

REFERENCES:

1. Xiaocong Fan, “Real-Time Embedded Systems: Design Principles and Engineering Practices”, Elsevier, 2015.
2. Albert M. K. Cheng, “Real-Time Systems: Scheduling, Analysis, and Verification“, Wiley publishers, 2003.
3. P. A. Laplante," Real-Time Systems Design & Analysis", Willey, 2011.
4. Qing Li, "Real Time Concepts for Embedded Systems", Elsevier, 2011.

COURSE OUTCOMES:

At the end of the course, the student should be able to:

CO1: Infer the characteristics of real time system.

CO2:apply scheduling algorithms based on the application.

CO3: discuss about the programming language characteristics and tools of real time systems.

CO4:choose the appropriate real time communication protocols.

CO5:analyze the fault tolerance and evaluation techniques in real time systems.

Board of Studies (BoS) : 23rd BOS of ECE held on 13.07.2022

Academic Council: 19th Academic Council held on 29.09.2022

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CO2	H	H	H	H	H	H	M	M	M	M	M	M	H	H	H
CO3	H	H	H	H	H	H	M	M	M	M	M	M	H	H	H

CO4	H	H	H	H	H	H	M	M	M	M	M	M	H	H	H
CO5	H	H	H	H	H	H	M	M	M	M	M	M	H	H	H

Note: L- Low Correlation M - Medium Correlation H -High Correlation

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.
Statement: Understanding of the real time systems will bring practical knowledge on quality education.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation
Statement: capable of promoting industrialization through the application of real-time system design principles.

ECEY 081	MULTICORE ARCHITECTURE	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To define the fundamentals in design and analysis of processor architecture.

COB2: To explain data level parallelism.

COB3: To interpret parallelism in threads.

COB4: To discuss about warehouse scale architectures.

COB5: To outline the GPU architecture.

PREREQUISITES: Computer Architecture, Processor design

MODULE I FUNDAMENTALS OF QUANTITATIVE DESIGN AND ANALYSIS **9**

Classes of Computers – Trends in Technology, Power, Energy and Cost – Dependability – Measuring, Reporting and Summarizing Performance – Quantitative Principles of Computer Design – Classes of Parallelism - ILP, DLP, TLP and RLP - Multithreading - SMT and CMP Architectures – Limitations of Single Core Processors

MODULE II DLP IN VECTOR AND SIMD **9**

Vector Architecture - SIMD Instruction Set Extensions for Multimedia – Graphics Processing Units - Detecting and Enhancing Loop Level Parallelism - Case Studies.

MODULE III TLP AND MULTIPROCESSORS **9**

Symmetric and Distributed Shared Memory Architectures – Cache Coherence Issues - Performance Issues – Synchronization Issues – Models of Memory Consistency - Interconnection Networks – Buses, Crossbar and Multi-stage Interconnection Networks.

MODULE IV RLP AND DLP IN WAREHOUSE-SCALE ARCHITECTURES **9**

Programming Models and Workloads for Warehouse - Scale Computers – Architectures for Warehouse - Scale Computing – Physical Infrastructure and Costs – Cloud Computing

MODULE V GPU ARCHITECTURE 9

Evolution of GPU architectures – Understanding Parallelism with GPU –Typical GPU Architecture – CUDA Hardware Overview – Threads, Blocks, Grids, Warps, Scheduling – Memory Handling with CUDA: Shared Memory, Global Memory, Constant Memory and Texture Memory.

L –45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. Shane Cook, CUDA Programming: —A Developer's Guide to Parallel Computing with GPUs (Applications of GPU Computing), First Edition, Morgan Kaufmann, 2012.
2. David R. Kaeli, Perhaad Mistry, Dana Schaa, Dong Ping Zhang, —Heterogeneous computing with OpenCL, 3rd Edition, Morgan Kauffman, 2015.

REFERENCES:

1. John L. Hennessey and David A. Patterson, "Computer Architecture – A Quantitative Approach", Morgan Kaufmann / Elsevier, 5th edition, 2012.
2. Kai Hwang, "Advanced Computer Architecture", Tata McGraw-Hill Education, 2003,
3. Richard Y. Kain, "Advanced Computer Architecture a Systems Design Approach", Prentice Hall, 2011.
4. Nicholas Wilt, —CUDA Handbook: A Comprehensive Guide to GPU Programming, Addison – Wesley, 2013.
5. Jason Sanders, Edward Kandrot, —CUDA by Example: An Introduction to General Purpose GPU Programming, Addison – Wesley, 2010.
6. David B. Kirk, Wen-mei W. Hwu, Programming Massively Parallel Processors – A Hands-on Approach, Third Edition, Morgan Kaufmann, 2016.

COURSE OUTCOMES:

At the end of the courses, the students will be able to

CO1: explain the basics of quantitative design and analysis of processor architecture.

CO2: illustrate data level parallelism in vector architecture.

CO3: discuss about thread level parallelism and multiprocessor issues.

CO4: analyze the performance of warehouse scale computing.

CO5: estimate the performance of the GPU.

Board of Studies (BoS) :
23rd BOS of ECE held on 13.07.2022

Academic Council:
19th Academic Council held on 29.09.2022

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CO1	M	M				M		L	L		M	H			H
CO2	M	M				M		L	L		M	H			H
CO3	M	M				M		L	L		M	H			H
CO4	M	M				M		L	L		M	H			H
CO5	M	M				M		L	L		M	H			H

Note: L- Low Correlation M - Medium Correlation H - High Correlation

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.
Statement:
Understanding of the course will bring a global impact on quality education.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation
Statement: Knowledge of this course will enhance skills to develop applications using multicore architecture in automotive industry.

ECEY 082	EMBEDDED SYSTEM FOR ROBOTICS	L	T	P	C
SDG: 4,8,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To apply the different types of sensors and actuators for robotic applications.

COB2: To analyze the concept of controlling, multitasking and configuration in robot design.

COB3: To classify the kinematic models of robotics.

COB4: To design the appropriate type of mobile robots.

COB5: To evaluate the performance of mobile robots for various applications.

PREREQUISITES: Knowledge on Embedded Systems and Robotics

MODULE I SENSORS AND ACTUATORS FOR ROBOTIC APPLICATIONS **9**

Sensors - Sensor Categories, Binary Sensor, Analog versus Digital Sensors, Shaft Encoder; A/D Converter, Position Sensitive Device; Compass, Gyroscope, Accelerometer, Inclinometer, Digital Camera. Actuators - DC Motors, H-Bridge, Pulse Width Modulation, Stepper Motors, Servos.

MODULE II CONTROL ELEMENTS, MULTITASKING AND COMMUNICATION MODEL **10**

Control - On-Off Control, PID Control, Velocity Control and Position Control, Multiple Motors – Driving Straight, V-Omega Interface. Multitasking - Cooperative Multitasking, Pre-emptive Multitasking, Synchronization, Scheduling, Interrupts and Timer-Activated Tasks; Wireless Communication - Communication Model, Messages, Fault-Tolerant Self-Configuration, User Interface and Remote Control, Sample Application Program.

MODULE III ROBOT KINEMATICS **9**

Evolution of robotics, Robot anatomy, Design and control issues, Manipulation and Control. Direct Kinematic Model – Denavit - Hartenberg Notation, Kinematic Relationship between adjacent links, Manipulator Transformation Matrix; Inverse Kinematic Model.

MODULE IV INTRODUCTION TO MOBILE ROBOT DESIGN 9

Driving Robots, Omni-Directional Robots, Balancing Robots, Walking Robots, Autonomous Planes, Autonomous Vessels and Underwater Vehicles, Robot Manipulators, Mobile Robot Simulation.

MODULE V MOBILE ROBOT APPLICATIONS 8

Localization and Navigation - Maze Exploration - Map Generation - Real-Time Image Processing - Automotive Systems.

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. Thomas Bräunl, “Embedded Robotics: Mobile Robot Design and Applications with Embedded Systems”, Third Edition, Springer-Verlag Berlin Heidelberg, 2008.
2. Nilanjan Dey, Amartya Mukherjee, “Embedded Systems and Robotics with Open Source Tools” CRC Press, 2016.

REFERENCES:

1. R.K.Mittal and I.J.Nagrath, “Robotics and Control”, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2003.
2. John J. Craig, “Introduction to Robotics: Mechanics and Control”, Third Edition, Pearson/Prentice Hall, 2005.
3. AnisKoubaa, "Robot Operating System (ROS) the Complete Reference”, First Volume, Springer, 2016.
4. Morgan Quigley, Brian Gerkey, and William D. Smart, “Programming Robots with ROS”, O’Reilly, 2015.

COURSE OUTCOMES:

On completion of the course, students will be able to

CO1: identify the types of sensors and actuators for robotic applications.

CO2: discuss about the control elements and communication interfaces for various robot designs.

CO3: explain the mechanical structure and kinematic model in robotics.

CO4: describe the different types of mobile robot design.

CO5: apply the use of mobile robots for different applications.

Board of Studies (BoS) :	**Academic Council:**
23rd BOS of ECE held on 13.07.2022	19th Academic Council held on 29.09.2022

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CO1	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO2	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO3	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO4	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H
CO5	H	H	H	H	L	L	L	M	M	M	M	M	H	H	H

Note: L- Low Correlation M -Medium Correlation H -High Correlation

SDG 4: Quality Education.
Statement: This course explains the various elements and methods for designing mobile robots which intend to provide quality education.

SDG 8: Apply finest Engineering minds and develop new technologies.
Statement: Development and use of new methods for robotic design provides sustainable economic growth and productive employment.

SDG 9: Industry, Innovation and Infrastructure
Statement: This course will deliver the concepts to design and innovate different types of robots which will enhance quality oflife and to meet industry requirements.

ECEY 085	EMBEDDED AUTOMOTIVE SYSTEMS	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: To define the fundamentals of automotive electronics.

COB2: To discuss the communication protocols in automotive systems.

COB3: To develop automotive embedded systems.

COB4: To interpret new trends in automotive industry.

COB5: To develop knowledge on AUTOSAR architectures.

PREREQUISITES: Embedded Networking, Automotive Systems

MODULE I ELECTRONICS IN AUTOMOBILE 10

Introduction- Body and convenience electronics: vehicle power supply controllers and lighting MODULEs, door control MODULEs, Safety electronics: active safety systems: ABS, ASR, ESP, passive safety systems: Restraint systems and their associated sensors in an automobile. Power train Electronics: Gasoline engine management, Infotainment electronics: Dashboard/instrument cluster, car audio, telematics systems, navigation systems, multimedia systems, cross application technologies.

MODULE II AUTOMOTIVE COMMUNICATION PROTOCOLS 9

CAN bus - Concepts of bus access and arbitration - Error processing and management - Definitions of the CAN protocol: 'ISO 11898-1' - Errors: their intrinsic properties, detection and processing – Physical layer, Application layers and development tools for CAN – LIN - Basic concept of the LIN 2.0 protocol.

FlexRay - Event-triggered and time-triggered aspects - TTCAN – Time-triggered communication on CAN- Towards high-speed, X-by-Wire and redundant systems-FlexRay

MODULE III AUTOMOTIVE EMBEDDED SYSTEMS 9

Automotive Embedded systems. Microcontroller in Automobile applications - Different Types of Microcontrollers in Automotive systems – Challenges in ECU design - Growth in the Automobile – Application in Vehicle Control - Power train - Driver Information – Steering – Telematics

MODULE IV DRIVE BY WIRE 9

Challenges and opportunities of X-by-wire: system & design requirements, steer-

by-wire, brake- by-wire, suspension-by-wire, gas-by-wire, power-by-wire, shift by wire. Future of Automotive Electronics.

MODULE V AUTOSAR 8

AUTOSAR Architecture- Basic concepts- Software components - Layered Architecture - Microcontroller Abstraction Layer – ECU Abstraction Layer - Complex Device Driver - Service Layer – RTE - Application Layer - Basic Software MODULEs – Diagnostics - Methodology - Tools in SW development using AutoSAR- EB tresos Studio.

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. D.Paret, “Multiplexed Networks for Embedded Systems”, John Wiley & Sons, 2014.
2. Marco Di Natale, Haibo Zeng, Paolo Giusto, ArkadebGhosal, “Understanding and Using the Controller Area Network Communication Protocol “, Springer publishers, 2012.

REFERENCES:

1. Konrad Etschberger, ”Controller Area Network: Basics, Protocols, Chips and Application”, IXXAT Press, 2001.
2. GlafP. Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”, Embedded System Academy, 2008.

COURSE OUTCOMES:

At the end of the courses, the students will be able to

CO1: design automotive embedded systems.

CO2: analyze various embedded products used in automotive industry.

CO3:illustrate CAN and LIN protocol

CO4:evaluate the opportunities involving technology, a product or a service required for developing a start-up idea used for automotive applications

CO5: analyze the features of AUTOSAR Architecture.

Board of Studies (BoS) :	**Academic Council:**
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CO2	H	H	H	M	H	L	L	L	L	L	L	L	H	H	H
CO3	H	H	H	M	H	L	L	L	L	L	L	L	H	H	H
CO4	H	H	H	M	H	L	L	L	L	L	L	L	H	H	H
CO5	H	H	H	H	H	L	L	L	L	L	L	L	H	H	H

Note: L- Low Correlation M -Medium Correlation H -High Correlation

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.

Statement:

Understanding of the course will bring a global impact on quality education.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation

Statement: Able to apply embedded automotive systems for industrial automation.

ECEY 086	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	L	T	P	C
SDG: 4,9		3	0	0	3

COURSE OBJECTIVES:

COB1: Define the root causes for Electromagnetic Noise (EMI), its sources.
COB2: Classify the effects of EMI and the required precautions to be taken/to be discussed with his peer group.
COB3: Analyze different measurement techniques of EMI
COB4: Estimate EMI standards for different applications
COB5: To choose various EMI testing methods

PREREQUISITES: Basics of Electromagnetic fields

MODULE I BASIC THEORY 10

Intra and inter system EMI, Elements of Interference: Conducted and Radiated EMI emission and susceptibility, EMC Engineering Application.

MODULE II COUPLING MECHANISM 9

Coupling paths, Coupling via the supply network, Common mode coupling, Differential mode coupling, Impedance coupling, Radiative coupling, Ground loop coupling, Cable related emissions and coupling, Transient sources, Automotive transients. Categorization of the electromagnetic interference: emission, susceptibility, transients, crosstalk, shielding and compatibility, signal integrity.

MODULE III EMI MITIGATION TECHNIQUES 9

Working principle of Shielding, LF Magnetic shielding, Apertures and shielding effectiveness, Choice of Materials for H, E, and free space fields, Gasketting and sealing, PCB Level shielding, Principle of Grounding.

MODULE IV STANDARDS AND REGULATION 9

Need for Standards, EMI Standardizing for different application. IEC, ANSI, FCC, AS/NZS, CISPR, BSI, CENELEC, ACEC. MIL461E

MODULE V EMI TEST METHODS AND INSTRUMENTATION 8

Fundamental considerations, EMI Shielding effectiveness tests, Open field test, TEM cell for immunity test, Shielded chamber , Shielded anechoic chamber, EMI test receivers, Spectrum analyzer, EMI test wave simulators, EMI coupling networks, Line impedance stabilization networks, Feed through capacitors, Antennas, Current probes.

L – 45 ; TOTAL HOURS – 45

TEXT BOOKS:

1. Henry W. Ott, “Electromagnetic Compatibility Engineering”, John Wiley & Sons Inc, Newyork, 2009.
2. Daryl Gerke and William Kimmel, “EDNs Designers Guide to Electromagnetic Compatibility”, Elsevier Science & Technology Books, 2002.
3. W Scott Bennett, “Control and Measurement of Unintentional Electromagnetic Radiation”, John Wiley & Sons Inc., (Wiley Interscience Series) 1997.

REFERENCES:

1. Dr Kenneth L Kaiser, “The Electromagnetic Compatibility Handbook”, CRC Press, 2005.
2. Paul, C.R., “Introduction to Electromagnetic Compatibility”, 2nd ed., Wiley, 2010.
3. David K. Cheng, “Field and Wave Electromagnetics”, 2nd ed. Pearson Education, 2009.

COURSE OUTCOMES:

At the end of the courses, the students will be able to

CO1: Classify effects of EMI and counter measures by EMC-techniques.

CO2: Select the proper gadget/device/appliance/system, as per EMC-norms specified by the regulating authorities.

CO3: To analyze coupling mechanisms

CO4: To develop systems with EMI standards

CO5: To choose career in the fields of EMI/EMC as an Engineer/Researcher

Board of Studies (BoS) : 23rd BOS of ECE held on 13.07.2022

Academic Council: 19th Academic Council held on 29.09.2022

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CO2	H	H	H	M	H	L	L	L	L	L	L	L	H	H	H
CO3	H	H	H	M	H	L	L	L	L	L	L	L	H	H	H
CO4	H	H	H	M	H	L	L	L	L	L	L	L	H	H	H
CO5	H	H	H	H	H	L	L	L	L	L	L	L	H	H	H

Note: L- Low Correlation M -Medium Correlation H - High Correlation

SDG 4: Ensure inclusive and equitable quality education and promote lifelong learning opportunities for all.
Statement: To implement EMI standards in industrial applications.

SDG 9: Build resilient Infrastructure, promote inclusive and sustainable industrialization and foster innovation
Statement: Apply different measurement techniques of EMI.