B.S. Abdur Rahman Crescent Institute of Science & Technology

Deemed to be University u/s 3 of the UGC Act, 1956

Regulations 2019
Curriculum and Syllabi

(Amendments updated upto June 2020)

M.Tech.
(VLSI & Embedded Systems)

B.S. Abdur Rahman Crescent Institute of Science & Technology
Deemed to be University u/s 3 of the UGC Act, 1956

REGULATIONS 2019
CURRICULUM AND SYLLABI
(Amendments updated upto June 2020)

M.TECH.
VLSI & EMBEDDED SYSTEMS

VISION AND MISSION OF THE INSTITUTION

VISION

B.S.Abdur Rahman Crescent Institute of Science and Technology aspires to be a leader in Education, Training and Research in multidisciplinary areas of importance and to play a vital role in the Socio-Economic progress of the Country in a sustainable manner.

MISSION

- To blossom into an internationally renowned Institute.
- To empower the youth through quality and value-based education.
- To promote professional leadership and entrepreneurship.
- To achieve excellence in all its endeavors to face global challenges.
- To provide excellent teaching and research ambience.
- To network with global Institutions of Excellence, Business, Industry and Research Organizations.
- To contribute to the knowledge base through Scientific enquiry, Applied Research and Innovation.

VISION AND MISSION OF THE DEPARTMENT OFELECTRONICS AND COMMUNICATION ENGINEERING

VISION

The Department of Electronics and Communication Engineering envisions to be a leader in providing state of the art education through excellence in teaching, training, and research in contemporary areas of Electronics and Communication Engineering and aspires to meet the global and socio economic challenges of the country.

MISSION

- The Department of Electronics and Communication Engineering, endeavours to produce globally competent Engineers prepared to face challenges of the society.
- To enable the students to formulate, design and solve problems in applied science and engineering.
- To provide excellent teaching and research environment using state of the art facilities.
- To provide adequate practical training to meet the requirement of the Electronics & communication industry.
- To train the students to take up leadership roles in their career or to pursue higher education and research.

PROGRAMME EDUCATIONAL OBJECTIVES AND OUTCOMES

M.Tech. (VLSI & EMBEDDED SYSTEMS)

PROGRAMME EDUCATIONAL OBJECTIVES:

The OBJECTIVES of the program is

PEO 1 To educate and train the graduates with knowledge and skills necessary to formulate, design and solve problems in Analog, Digital & Mixed Signal VLSI system design, VLSI Signal Processing, Real Time Embedded System design and Hardware Software Co-Design

PEO 2 To provide technical skills in software and hardware tools related to the design and implementation of integrated Circuits, System on Chip for real time applications

PEO 3 To provide scope for Applied Research and innovation in the various fields of VLSI and Embedded Systems, and enabling the students to work in the emerging areas

PEO 4 To enhance communication and soft skills of students to make them work effectively as a team

PROGRAMME OUTCOMES:

On successful completion of the programme, the graduates will be able to

- Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- Identify, formulate, research literature, and analyses complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- Use research –based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions.

- Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
- Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

PROGRAMME SPECIFIC OUTCOMES

On successful completion of the programme, the graduates will

PO1 Be able to analyze, design and implement Analog, Digital and Mixed Signal Circuits and real time embedded systems

PO2 Have in-depth knowledge and capability to use industry standard tools in the design and implementation of VLSI and real time Embedded Systems.

PO3 Be able to undertake research projects in related domains of VLSI and Embedded systems.

PO4 Possess the capability to communicate effectively and work as a team in the professional career

B.S. ABDUR RAHMAN CRESCENT INSTITUTE OF SCIENCE & TECHNOLOGY, CHENNAI – 600 048.

REGULATIONS - 2019 FOR

M.Tech. / MCA / M.Sc. DEGREE PROGRAMMES

(Under Choice Based Credit System)

1.0 PRELIMINARY DEFINITIONS AND NOMENCLATURE

In these Regulations, unless the context otherwise requires **"Programme"** means Post Graduate Degree Programme (M.Tech. / MCA / M.Sc.)

"Course" means a theory / practical / laboratory integrated theory / mini project / seminar / internship / Project and any other subject that is normally studied in a semester like Advanced Concrete Technology, Electro Optic Systems, Financial Reporting and Accounting, Analytical Chemistry, etc.,

"Institution" means B.S. Abdur Rahman Crescent Institute of Science & Technology.

"Academic Council" means the Academic Council, which is the apex body on all academic matters of B.S. Abdur Rahman Crescent Institute of Science & Technology.

"Dean (Academic Affairs)" means Dean (Academic Affairs) of B.S. Abdur Rahman Crescent Institute of Science & Technology who administers the academic matters.

"Dean (Student Affairs)" means Dean (Student Affairs) of B.S. Abdur Rahman Crescent Institute of Science & Technology, who looks after the welfare and discipline of the students.

"Controller of Examinations" means the Controller of Examinations of B.S. Abdur Rahman Crescent Institute of Science & Technology who is responsible for the conduct of examinations and declaration of results.

2.0 PROGRAMMES OFFERED AND ADMISSION REQUIREMENTS

2.1 Programmes Offered

The various programmes and their mode of study are as follows:

Degree	Mode of Study
M.Tech.	Full Time
MCA	
M.Sc.	

2.2 ADMISSION REQUIREMENTS

2.2.1 Students for admission to the first semester of the Master's Degree Programme shall be required to have passed the appropriate degree examination of this Institution as specified in the clause 3.2 [Eligible entry qualifications for admission to P.G. programmes] or any other degree examination of any University or authority accepted by this Institution as equivalent thereto.

2.2.2 Eligibility conditions for admission such as class obtained, number of attempts in the qualifying examination and physical fitness will be as prescribed by the Institution from time to time.

3.0 DURATION, ELIGIBILITY AND STRUCTURE OF THE PROGRAMME

3.1. The minimum and maximum period for completion of the Programmes are given below:

Programme	Min. No. of Semesters	Max. No. of Semesters
M.Tech.	4	8
MCA (3 years)	6	12
MCA (Lateral Entry)	4	8
MCA (2 years)	4	8
M.Sc.	4	8

3.1.1 Each academic semester shall normally comprise of 90 working days. Semester End Examinations shall follow within 10 days of the last Instructional day.

3.1.2 Medium of instruction, examinations and project report shall be in English.

3.2 ELIGIBLE ENTRY QUALIFICATIONS FOR ADMISSION TO PROGRAMMES

Sl. No.	Name of the Department	Programmes offered	Qualifications for admission
1.	Aeronautical Engineering	M. Tech. (Avionics)	B.E. / B. Tech. (Aeronautical Engineering)
2.	Civil Engineering	M. Tech. (Structural Engineering)	B.E. / B. Tech. (Civil Engineering) / (Structural Engineering)

		M. Tech. (Construction Engineering and Project Management)	B.E. / B. Tech. (Civil Engineering) / (Structural Engineering) / B. Arch.
3.	Mechanical Engineering	M.Tech. (Manufacturing Engineering)	B.E. / B.Tech. (Mechanical / Automobile / Manufacturing / Production / Industrial / Mechatronics / Metallurgy / Aerospace /Aeronautical / Material Science / Marine Engineering)
		M.Tech. (CAD/CAM)	
4.	Electrical and Electronics Engineering	M.Tech. (Power Systems Engg.)	B.E. / B. Tech. (EEE/ECE/E&I/I&C / Electronics / Instrumentation)
		M.Tech. (Power Electronics and Drives)	
5.	Electronics and Communication Engineering	M.Tech. (Communication Systems)	B.E. / B. Tech. (EEE/ ECE / E&I / CSE IT / I&C / Electronics / Instrumentation)
		M.Tech. (VLSI and Embedded Systems)	B.E. / B. Tech. (ECE / E&I / I&C / EEE / CSE / IT)
6.	Electronics and Instrumentation Engineering	M.Tech. (Electronics and Instrumentation Engineering)	B.E. / B. Tech. (EIE/ICE/Electronics/ECE/EEE)
7.	Computer Science and Engineering	M.Tech. (Computer Science and Engineering)	B.E. / B. Tech. (CSE/IT/ECE/EEE/EIE/ICE/ Electronics / MCA)
8.	Information Technology	M.Tech. (Information Technology)	B.E. / B. Tech. (IT/CSE/ECE/EEE/EIE/ICE/ Electronics / MCA)

9.	Computer Applications	MCA (3 years)	Bachelor Degree in any discipline with Mathematics as one of the subjects (or) Mathematics at +2 level
		MCA – (Lateral Entry)	B.Sc. Computer Science / B.Sc. Information Technology / BCA
		MCA (2 years)	Bachelor Degree in any discipline with Mathematics as one of the subjects (or) Mathematics at +2 level or B.Sc. Computer Science / B.Sc. Information Technology / BCA
10.	Mathematics	M.Sc. (Actuarial Science)	Any Degree with Mathematics / Statistics as one of the subjects of study
11.	Physics	M.Sc.(Physics)	B.Sc. (Physics / Applied Science / Electronics / Electronics Science / Electronics & Instrumentation)
12.	Chemistry	M.Sc.(Chemistry)	B.Sc. (Chemistry / Applied Science)
13.	Life Sciences	M.Sc. Molecular Biology & Biochemistry	B.Sc. in any branch of Life Sciences
		M.Sc. Biotechnology	B.Sc. in any branch of Life Sciences
		M.Sc. Microbiology	B.Sc. in any branch of Life Sciences
		M.Tech. Biotechnology	B.Tech. (Biotechnology / Chemical Engineering) / M.Sc. in any branch of Life Sciences

3.3. STRUCTURE OF THE PROGRAMME

3.3.1 The PG. programmes consist of the following components as prescribed in

the respective curriculum

i. Core courses
ii. Elective courses
iii. Laboratory oriented core courses
iv. Project work / thesis / dissertation
v. Laboratory Courses
vi. Seminars
vii. Mini Project
viii. Industrial Internship
ix. Value Added Courses
x. MOOC Courses (NPTEL, SWAYAM, etc.,)

3.3.2 The curriculum and syllabi of all programmes shall be approved by the Academic Council of this Institution.

3.3.3 For the award of the degree, the student has to earn a minimum total credits specified in the curriculum of the respective specialization of the programme.

3.3.4 The curriculum of programmes shall be so designed that the minimum prescribed credits required for the award of the degree shall be within the limits specified below:

Programme	Range of credits
M.Tech.	74 - 80
MCA (3 years)	118 - 126
MCA (Lateral Entry)	80 - 85
MCA (2 years)	85 - 90
M.Sc.	77- 82

3.3.5 Credits will be assigned to the courses for all programmes as given below:

- One credit for one lecture period per week or 15 periods of lecture per semester
- One credit for one tutorial period per week or 15 periods per semester
- One credit each for seminar/practical session/project of two or three periods per week or 30 periods per semester
- One credit for four weeks of industrial internship or 160 hours per semester.

3.3.6 The number of credits the student shall enroll in a non-project semester and

project semester is as specified below to facilitate implementation of Choice Based Credit System.

Programme	Non-project semester	Project semester
M.Tech.	9 to 28	18 to 26
MCA	12 to 33	12 to 26
M.Sc.	9 to 32	10 to 26

3.3.7 The student may choose a course prescribed in the curriculum from any department offering that course without affecting regular class schedule. The attendance will be maintained course wise only.

3.3.8 The students shall choose the electives from the curriculum with the approval of the Head of the Department / Dean of School.

3.3.9 Apart from the various elective courses listed in the curriculum for each specialization of programme, the student can choose a maximum of two electives from any other similar programmes across departments, during the entire period of study, with the approval of the Head of the department offering the course and parent department.

3.4. ONLINE COURSES

3.4.1 Students are permitted to undergo department approved online courses under SWAYAM up to 20% of credits of courses in a semester excluding project semester with the recommendation of the Head of the Department / Dean of School and with the prior approval of Dean Academic Affairs during his/ her period of study. The credits earned through online courses ratified by the respective Board of Studies shall be transferred following the due approval procedures. The online courses can be considered in lieu of core courses and elective courses.

3.4.2 Students shall undergo project related online course on their own with the mentoring of the faculty member.

3.5 PROJECT WORK / DISSERTATION

3.5.1 Project work / Dissertation shall be carried out by the student under the supervision of a Faculty member in the department with similar specialization.

3.5.2 A student may however, in certain cases, be permitted to work for the project in an Industry / Research Organization, with the approval of the Head of the Department/ Dean of School. In such cases, the project work shall be jointly

supervised by a faculty of the Department and an Engineer / Scientist from the organization and the student shall be instructed to meet the faculty periodically and to attend the review meetings for evaluating the progress.

3.5.3 The timeline for submission of final project report / dissertation is within 30 calendar days from the last Instructional day of the semester in which Project / Dissertation is done.

3.5.4 If a student does not comply with the submission of project report / dissertation on or before the specified timeline he / she is deemed to have not completed the project work / dissertation and shall re-register in the subsequent semester.

4.0 CLASS ADVISOR AND FACULTY ADVISOR

4.1 CLASS ADVISOR

A faculty member shall be nominated by the HOD / Dean of School as Class Advisor for the whole class. He/she is responsible for maintaining the academic, curricular and co-curricular records of all students throughout their period of study.

4.2 FACULTY ADVISOR

To help the students in planning their courses of study and for general counseling on the academic programme, the Head of the Department / Dean of School of the students shall attach a certain number of students to a faculty member of the department who shall function as Faculty Advisor for the students throughout their period of study. Such Faculty Advisor shall offer advice to the students on academic and personal matters, and guide the students in taking up courses for registration and enrolment in every semester.

5.0 CLASS COMMITTEE

5.1 A class committee comprising faculty members handling the classes, student representatives and a senior faculty member not handling the courses as chairman will be constituted in every semester:

5.2 The composition of the class committee will be as follows:

i) One senior faculty member preferably not handling courses for the concerned semester, appointed as chairman by the Head of the Department

ii) Faculty members of all courses of the semester

iii) All the students of the class

iv) Faculty advisor and class advisor

v) Head of the Department – Ex officio member

5.3 The class committee shall meet at least three times during the semester. The first meeting shall be held within two weeks from the date of commencement of classes, in which the nature of continuous assessment for various courses and the weightages for each component of assessment shall be decided for the first and second assessment. The second meeting shall be held within a week after the date of first assessment report, to review the students' performance and for follow up action.

5.4 During these two meetings the student members, shall meaningfully interact and express opinions and suggestions to improve the effectiveness of the teaching-learning process, curriculum and syllabus.

5.5 The third meeting of the class committee, excluding the student members, shall meet within 5 days from the last day of the semester end examination to analyze the performance of the students in all the components of assessments and decide their grades in each course. The grades for a common course shall be decided by the concerned course committee and shall be presented to the class committee(s) by the concerned course coordinator.

6.0 COURSE COMMITTEE

6.1 Each common theory / laboratory course offered to more than one group of students shall have a “Course Committee” comprising all the teachers handling the common course with one of them nominated as course coordinator. The nomination of the course coordinator shall be made by the Head of the Department / Dean (Academic Affairs) depending upon whether all the teachers handling the common course belong to a single department or from several departments. The Course Committee shall meet as often as possible to prepare a common question paper, scheme of evaluation and ensure uniform evaluation of the assessment tests and semester end examination.

7.0 REGISTRATION AND ENROLLMENT

7.1 The students of first semester shall register and enroll at the time of admission by paying the prescribed fees.

7.2 For the subsequent semesters registration for the courses shall be done by the student one week before the last working day of the previous semester.

7.3 A student can withdraw from an enrolled course at any time before the first assessment test for genuine reasons, with the approval of the Dean (Academic Affairs), on the recommendation of the Head of the Department of the student.

7.4 A student can change an enrolled course within 10 working days from the commencement of the course, with the approval of the Dean (Academic Affairs), on the recommendation of the Head of the Department of the student.

8.0 TEMPORARY BREAK OF STUDY FROM THE PROGRAMME

8.1 A student may be permitted by the Dean (Academic Affairs) to avail temporary break of study from the programme up to a maximum of two semesters for reasons of ill health or other valid grounds. A student can avail the break of study before the start of first assessment test of the ongoing semester. However the total duration for completion of the programme shall not exceed the prescribed maximum number of semesters (vide clause 3.1). If any student is debarred for want of attendance or suspended due to any act of indiscipline, it will not be considered as break of study. A student who has availed break of study has to rejoin in the same semester only in the subsequent year. The student availing break of study is permitted to write arrear examinations by paying the prescribed fees.

9.0 MINIMUM REQUIREMENTS TO REGISTER FOR PROJECT / DISSERTATION

9.1 A student is permitted to register for project semester, if he/she has earned the minimum number of credits specified below:

Programme	**Minimum no. of credits to be earned to enroll for project semester**
M.Tech.	18
MCA (3 years)	45
MCA (Lateral Entry)	22
MCA (2 years)	22

M.Sc.	18

9.2 If the student has not earned minimum number of credits specified, he/she has to earn the required credits, at least to the extent of minimum credits specified in clause 9.1 and then register for the project semester.

10.0 ATTENDANCE

10.1 A student shall earn 100% attendance in the contact periods of every course, subject to a maximum relaxation of 25% (for genuine reasons such as medical grounds, representing for the institution in approved events, etc.) to become eligible to appear for the semester end examination in that course, failing which the student shall be awarded "I" grade in that course. The courses in which the student is awarded "I" grade, shall register and redo the course when it is offered next.

10.2 The faculty member of each course shall cumulate the attendance details for the semester and furnish the names of the students who have not earned the required attendance in that course to the Class Advisor. The Class Advisor will consolidate and furnish the list of students who have earned less that 75% attendance, in various courses, to the Dean (Academic Affairs) through the Head of the Department / Dean of School. Thereupon, the Dean (Academic Affairs) shall announce the names of such students prevented from writing the semester end examination in each course.

10.3 A student who has obtained 'I' grade in all the courses in a semester is not permitted to move to next higher semester. Such student shall redo all the courses of the semester in the subsequent academic year. However he / she is permitted to redo the courses awarded with 'I' grade / arrear in previous semesters. They shall also be permitted to write arrear examinations by paying the prescribed fee.

10.4 A student shall register to redo a core course wherein "I" or "W" grade is awarded. If the student is awarded, "I" or "W" grade in an elective course either the same elective course may be repeated or a new elective course may be chosen with the approval of Head of the Department / Dean of School.

11.0 REDO COURSES

11.1 A student can register for a maximum of two redo courses per semester in the

evening after regular working hours, if such courses are offered by the concerned department. Students may also opt to redo the courses offered during regular semesters, without affecting the regular academic schedule and not exceeding prescribed maximum credits.

11.2 The Head of the Department with the approval of Dean (Academic Affairs) may arrange for the conduct of a few courses in the evening after regular working hours, depending on the availability of faculty members and subject to a specified minimum number of students registering for each of such courses.

11.3 The number of contact hours and the assessment procedure for any redo course will be the same as those during regular semesters except that there is no provision for any substitute examination and withdrawal from an evening redo course.

12.0 ASSESSMENTS AND EXAMINATIONS

12.1 Every theory course shall have a total of three assessments during a semester as given below:

Assessments	Weightage of Marks
Continuous Assessment 1	25%
Continuous Assessment 2	25%
Semester End Examination	50%

12.2 Appearing for semester end theory examination for each course is mandatory and a student should secure a minimum of 40% marks in each course in semester end examination for the successful completion of the course.

Every practical course shall have 75% weightage for continuous assessments and 25% for semester end examination. However a student should have secured a minimum of 50% marks in the semester end practical examination for the award of pass grade.

12.3 For laboratory integrated theory courses, the theory and practical components shall be assessed separately for 100 marks each and consolidated by assigning a weightage of 75% for theory component and 25% for practical component. Grading shall be done for this consolidated mark. Assessment of theory component shall have a total of three assessments with two continuous assessments having 25% weightage each and semester end examination

having 50% weightage. The student shall secure a separate minimum of 40% in the semester end theory examination for the award of pass grade. The evaluation of practical component shall be through continuous assessment.

12.4 The components of continuous assessment for theory/practical/laboratory integrated theory courses shall be finalized in the first class committee meeting.

12.5 In the case of Industrial training, the student shall submit a report, which shall be evaluated along with an oral examination by a committee of faculty members constituted by the Head of the Department. The student shall also submit an internship completion certificate issued by the industry / research organisation. The weightage for Industry internship report shall be 60% and 40% for viva voce examination.

12.6 In the case of project work, a committee of faculty members constituted by the Head of the Department will carry out three periodic reviews. Based on the project report submitted by the student, an oral examination (viva voce) shall be conducted as semester end examination by an external examiner approved by Controller of Examinations. The weightage for periodic reviews shall be 50%. Of the remaining 50%, 20% shall be for the project report and 30% for the Viva Voce examination.

12.7 For the first attempt of the arrear theory examination, the internal assessment marks scored for a course during first appearance shall be considered for grading along with the marks scored in the semester end arrear examination. From the subsequent appearance onwards, full weightage shall be assigned to the marks scored in the semester end examination to award grades and the internal assessment marks secured during the course of study shall not be considered.

In case of laboratory integrated theory courses, after one regular and one arrear appearance, the internal mark of theory component is invalid and full weightage shall be assigned to the marks scored in the semester end arrear examination for theory component. There shall be no arrear or improvement examination for lab component.

13.0 SUBSTITUTE EXAMINATIONS

13.1 A student who is absent, for genuine reasons, may be permitted to write a

substitute examination for any one of the two continuous assessment tests of a course by paying the prescribed substitute examination fee. However, permission to take up a substitute examination will be given under exceptional circumstances, such as accidents, admission to a hospital due to illness, etc. by a committee constituted by the Head of the Department / Dean of School for that purpose. However there is no substitute examination for semester end examination.

13.2 A student shall apply for substitute exam in the prescribed form to the Head of the Department / Dean of School within a week from the date of assessment test. However the substitute examination will be conducted only after the last working day of the semester and before the semester end examination.

14.0 SUPPLEMENTARY EXAMINATION

14.1 Final Year students can apply for supplementary examination for a maximum of three courses thus providing an opportunity to complete their degree programme. Likewise students with less credit can also apply for supplementary examination for a maximum of three courses to enable them to earn minimum credits to move to higher semester. The students can apply for supplementary examination within three weeks of the declaration of results in both odd and even semester.

15. PASSING, DECLARATION OF RESULTS AND GRADE SHEET

15.1 All assessments of a course shall be made on absolute marks basis. However, the Class Committee without the student members shall meet within 5 days after the semester end examination and analyze the performance of students in all assessments of a course and award letter grades. The letter grades and the corresponding grade points are as follows:

Letter Grade	Grade Points
S	10
A	9
B	8
C	7
D	6
E	5
U	0

W	0
I	0
AB	0

"W" denotes withdrawal from the course.

"I" denotes inadequate attendance and hence prevented from appearing for semester end examination

"U" denotes unsuccessful performance in the course.

"AB" denotes absence for the semester end examination.

15.2 A student who earns a minimum of five grade points ('E' grade) in a course is declared to have successfully completed the course. Such a course cannot be repeated by the student for improvement of grade.

15.3 The results, after awarding of grades, shall be signed by the Chairman of the Class Committee and Head of the Department / Dean of School and it shall be declared by the Controller of Examinations.

15.4 Within one week from the date of declaration of result, a student can apply for revaluation of his / her semester end theory examination answer scripts of one or more courses, on payment of prescribed fee to the Controller of Examinations. Subsequently the Head of the Department/ Dean of School offered the course shall constitute a revaluation committee consisting of Chairman of the Class Committee as convener, the faculty member of the course and a senior faculty member knowledgeable in that course as members. The committee shall meet within a week to re-evaluate the answer scripts and submit its report to the Controller of Examinations for consideration and decision.

15.5 After results are declared, grade sheets shall be issued to each student, which contains the following details: a) list of courses enrolled during the semester including redo courses / arrear courses, if any; b) grades scored; c) Grade Point Average (GPA) for the semester and d) Cumulative Grade Point Average (CGPA) of all courses enrolled from first semester onwards.

GPA is the ratio of the sum of the products of the number of credits of courses registered and the grade points corresponding to the grades scored in those courses, taken for all the courses, to the sum of the number of credits of all the courses in the semester.

If C_i, is the number of credits assigned for the i^{th} course and GP_i is the Grade Point in the i^{th} course

$$GPA = \frac{\sum_{i=1}^{n}(C_i)(GPi)}{\sum_{i=1}^{n} C_i}$$

Where n = number of courses

The Cumulative Grade Point Average (CGPA) is calculated in a similar manner, considering all the courses enrolled from first semester.

“I” and "W" grades are excluded for calculating GPA.

"U", “I”, "AB" and **"W"** grades are excluded for calculating CGPA.

The formula for the conversion of CGPA to equivalent percentage of marks is as follows:

Percentage Equivalent of Marks = CGPA X 10

15.6 After successful completion of the programme, the Degree shall be awarded upon fulfillment of curriculum requirements and classification based on CGPA as follows:

Classification	CGPA
First Class with Distinction	8.50 and above and passing all the courses in first appearance and completing the programme within the minimum prescribed period.
First Class	6.50 and above and completing the programme within a minimum prescribed period plus two semesters.
Second Class	Others

However, to be eligible for First Class with Distinction, a student should not have obtained ‘U’ or ‘I’ grade in any course during his/her period of study and should have completed the P.G. programme within a minimum period (except break of study). To be eligible for First Class, a student should have passed the examination in all the courses within the specified minimum number of semesters reckoned from his/her commencement of study plus two semesters. For this purpose, the authorized break of study is not considered. The students who do not satisfy the above two conditions shall be classified as second class. For the purpose of classification, the CGPA shall be rounded to two decimal places. For the purpose of comparison of performance of students and ranking, CGPA will be considered up to three

decimal places.

16.0 DISCIPLINE

16.1 Every student is expected to observe disciplined and decorous behaviour both inside and outside the campus and not to indulge in any activity which tends to affect the reputation of the Institution.

16.2 Any act of indiscipline of a student, reported to the Dean (Student Affairs), through the HOD / Dean shall be referred to a Discipline and Welfare Committee constituted by the Registrar for taking appropriate action.

17.0 ELIGIBILITY FOR THE AWARD OF THE MASTERS DEGREE

17.1 A student shall be declared to be eligible for the award of the Masters Degree, if he/she has:

i. Successfully acquired the required credits as specified in the curriculum corresponding to his/her programme within the stipulated time.
ii. No disciplinary action is pending against him/her.
iii. Enrolled and completed at least one value added course.
iv. Enrollment in at least one MOOC / SWAYAM course (non-credit) before the final semester.

17.2 The award of the degree must have been approved by the Institute.

18.0 POWER TO MODIFY

Not withstanding all that have been stated above, the Academic Council has the right to modify any of the above regulations from time to time.

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B.S. ABDUR RAHMAN CRESCENT INSTITUTE OF SCIENCE AND TECHNOLOGY

CURRICULUM &SYLLABI FOR

M.Tech.(VLSI &EMBEDDED SYSTEMS)
(FOUR SEMESTERS / FULL TIME)

Sl. No.	Course Code	Course Title	L	T	P	C
		SEMESTER I				
1	MAD 6184	Probability Matrix Theory & Linear Programming	**3**	**1**	**0**	**4**
2	ECD 6121	Digital VLSI Design	**3**	**0**	**0**	**3**
3	ECD 6122	Advanced Embedded System and Programming	**3**	**0**	**0**	**3**
4	ECD 6123	CMOS Mixed Signal Circuit Design	**3**	**0**	**0**	**3**
5	ECD 6124	Advanced Microcontroller architecture and Programming	**3**	**0**	**2**	**4**
6	ECD 6125	VLSI Physical Design Automation Lab	**0**	**0**	**2**	**1**
7		Professional Elective (Minimum of 3 credits to be earned)				**3**
						21
		SEMESTER II				
Sl. No.	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	ECD 6201	Research Methodology for Engineers	**3**	**1**	**0**	**4**
2	ECD 6221	Real Time Operating Systems	**3**	**0**	**0**	**3**
3	ECD 6222	Analog Integrated Circuit Design	**3**	**0**	**2**	**4**
4	ECD 6223	Embedded System Laboratory	**0**	**0**	**2**	**1**
5		Professional Elective (Minimum of 9 credits to be earned)				**9**
6		Value added course	**0**	**0**	**0**	**0**
						21

SEMESTER III

Sl. No.	Course Code	Course Title	L	T	P	C
1	GED	General Elective	**3**	**0**	**0**	**3**
2	ECD 7121	Project Work - Phase I*	**0**	**0**	**12**	**6***
3	ECD 7122	Internship**	**0**	**0**	**2**	**1**
4		Professional Elective (Minimum of 6 credits to be earned)				**6**
5		MOOC (Related to project)	**0**	**0**	**0**	**0**
						10

SEMESTER IV

Sl. No.	Course Code	Course Title	L	T	P	C
1	ECD 7121	Project Work - Phase II*	**0**	**0**	**36**	**18***
						18 + 6 = 24

* Credits for Project Work Phase I to be accounted along with Project Work Phase II in IV Semester

** Internship has to be carried out at the end of second semester during summer vacation

Total Credits: 76

LIST OF PROFESSIONAL ELECTIVES- VLSI

Sl. No.	Course Code	Course Title	L	T	P	C
1	ECDY 051	CAD for VLSI Circuits	**3**	**0**	**0**	**3**
2	ECDY 052	ASIC Design	**3**	**0**	**0**	**3**
3	ECDY 053	Advanced Digital System Design	**3**	**0**	**0**	**3**
4	ECDY 054	MEMS System Design	**3**	**0**	**0**	**3**
5	ECDY 055	Optimization Techniques and their applications in VLSI design	**3**	**0**	**0**	**3**
6	ECDY 056	Programming Verilog HDL	**3**	**0**	**2**	**4**
7	ECDY 057	Reconfigurable Computing	**3**	**0**	**0**	**3**
8	ECDY 058	RF Integrated Circuits Design	**3**	**0**	**0**	**3**
9	ECDY 059	Semiconductor Memories	**3**	**0**	**0**	**3**
10	ECDY 060	SoC design and Verification	**3**	**0**	**0**	**3**
11	ECDY 061	Testing of VLSI Circuits	**3**	**0**	**0**	**3**
12	ECDY 062	VLSI Digital Signal Processing	**3**	**0**	**0**	**3**
13	ECDY 063	DSP System Design	**2**	**0**	**0**	**2**
14	ECDY 064	Electronic Design Automation Tools	**2**	**0**	**0**	**2**
15	ECDY 065	Programming System Verilog	**2**	**0**	**0**	**2**
16	ECDY 066	Scripting Languages for VLSI Design Automation	**1**	**0**	**0**	**1**

LIST OF PROFESSIONAL ELECTIVES- EMBEDDED SYSTEMS

Sl. No.	Course Code	Course Title	L	T	P	C
1	ECDY 025	Wireless Sensor Networks	3	0	0	3
2	ECDY 034	Software for Embedded Systems	2	0	2	3
3	ECDY 024	Internet of Things	3	0	0	3
4	ECDY 072	Controller Area Network	3	0	0	3
5	ECDY 073	Distributed Embedded Computing	3	0	0	3

6	ECDY 074	Embedded Networking	3	0	0	3
7	ECDY 075	Embedded LINUX	3	0	0	3
8	ECDY 076	Hardware-software co-design	3	0	0	3
9	ECDY 077	Real Time Systems	3	0	0	3
10	ECDY 078	RISC Processor Architecture and Programming	3	0	0	3
11	ECDY 079	Industrial Automation using PLC, DCS and SCADA	3	0	2	4
12	ECDY 080	Sensors Lab	0	0	2	1
13	ECDY 081	Multicore Architecture	3	0	0	3
14	ECDY 082	Embedded System for Robotics	3	0	0	3
15	ECDY 083	Network on chip	3	0	0	3
16	ECDY 084	Interoperability Challenges in Internet of Things	3	0	0	3
17	ECDY 085	Embedded Automotive System	3	0	0	3

GENERAL ELECTIVE

Sl. No.	Course Code	Course Title	L	T	P	C
1.	GEDY 101	Project Management	3	0	0	3
2.	GEDY 102	Society, Technology & Sustainability	3	0	0	3
3.	GEDY 103	Artificial Intelligence	3	0	0	3
4.	GEDY 104	Green Computing	3	0	0	3
5.	GEDY 105	Gaming Design	3	0	0	3
6.	GEDY 106	Social Computing	3	0	0	3
7.	GEDY 107	Soft Computing	3	0	0	3
8.	GEDY 108	Embedded System Programming	3	0	0	3
9.	GEDY 109	Principles of Sustainable Development	3	0	0	3
10.	GEDY 110	Quantitative Techniques in Management	3	0	0	3
11.	GEDY 111	Programming using MATLAB & SIMULINK	1	0	2	2
12.	GEDY 112	JAVA Programming	3	0	0	3

13.	GEDY 113	PYTHON Programming	3	0	0	3
14.	GEDY 114	Intellectual Property Rights	1	0	0	1

SEMESTER I

MAD 6184 PROBABILITY, MATRIX THEORY AND LINEAR PROGRAMMING

L	T	P	C
3	1	0	4

OBJECTIVES:

The aim of this course is to

- Introduce the concepts of a random variable and a probability distribution.
- Identify and handle the situations involving more than one random variable.
- Find the eigenvalues of a matrix using qr transformations.
- Find the optimum value or optimum utilization of the resources using the lpp techniques.
- Familiarize students with variational problems.

PREREQUISITES :

Students should have a good knowledge in

- Evaluating differentiation and integration
- Matrix operations

MODULE I PROBABILITY DISTRIBUTIONS 10+3

Axioms of probability – addition and multiplication theorem – conditional probability – total probability – random variables - moments – moments generating functions and their properties- Binomial, Poisson, Geometric, Uniform, Exponential and Normal distributions.

MODULE II TWO DIMENSIONAL RANDOM VARIABLES 8+3

Joint distributions - marginal and conditional distributions – functions of random variables - covariance - correlation and regression - Central limit theorem.

MODULE III ADVANCED MATRIX THEORY 9+3

Matrix norms – singular value decomposition – QR algorithm - pseudo inverse – least square approximations – Toeplitz matrices and some applications.

MODULE IV LINEAR PROGRAMMING 10+3

Formation – graphical method - simplex method – Big-M method – Two Phase method- transportation and assignment problems.

MODULE V CALCULUS OF VARIATIONS 8+3

Variation and its properties – Euler's equation – functional dependant on first and higher order derivatives – functional dependant on functions of several independent variables – variational problems with moving boundaries – isoperimetric problems – Ritz and Kantorovich methods.

L – 45; T – 15 Total Hours: 60

TEXT BOOK

1. S.M.Ross, "A First Course in Probability", 10th edition, Pearson Education, 2018.
2. Lewis.D.W., "Matrix Theory", Allied Publishers, Chennai, 1995.
3. Taha, H.A., "Operations Research - An Introduction ", 10th edition, Pearson Prentice Hall, 2016.
4. A.S.Gupta, "Calculus of variations with applications", PHI Pvt. Ltd, New Delhi, 2017.

REFERENCE BOOK

1. H. Cramer., "Random Variables and Probability Distributions", Cambridge University Press (2004).
2. Roger A. Horn, Charles R. Johnson, "Matrix Analysis", Cambridge University Press; 2 edition (2012).
3. Robert.J.Vanderbei., "Linear Programming: Foundations and Extensions", Springer US(2014).
4. David. J. Rader., "Deterministic Operations Research", Wiley (2010).
5. Elsgolts, "Differential Equations and Calculus of Variations", University Press of the Pacific (2003).

OUTCOMES :

At the end of the course, the student should be able to:

- Distinguish between discrete and continuous random variables.
- Solve real life problems using standard distributions.
- Solve algebraic eigen value problems.
- Analyse the LPP techniques in deriving the optimality for real life situations.
- Solve problems on calculus of variations
- Apply variational problems with moving boundaries and isoperimetric problems for real life situations.

ECD 6121	DIGITAL VLSI DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- Characterize the key delay quantities of a standard cell
- Evaluate power dissipated in a circuit (dynamic and leakage)
- Design a circuit to perform a certain functionality with specified speed
- Identify the critical path of a combinational circuit
- Convert the combinational block to pipelined circuit
- Calculate the maximum (worst case) operating frequency of the designed circuit

PREREQUISITES :

- VLSI Design, Basics of Electronic circuit theory

MODULE I THE MOS TRANSISTOR 10

Silicon and Doping, P-N Junction, CMOS Transistor, Threshold Voltage, ON Current, Channel length modulation, Velocity saturation, Sub-threshold leakage, Drain Induced Barrier Leakage, Gate Induced Drain leakage, (Reverse) Short Channel Effect, Other leakage mechanisms, CMOS Inverter - Static Characteristic, Dynamic Characteristic, Introduction to fabrication technologies – crystal growth, Wafer cleaning, Oxidation, Thermal Diffusion, Ion Implantation, Lithography, Epitaxy, Metallization, Dry and Wet etching and Packaging, Fabrication of MOSFET.

MODULE II CMOS LOGIC FAMILIES, COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS 9

Pass Transistors, Transmission Gates; Designing with transmission gates, Primitive Logic Gates; Complex Logic Circuits.SR Latch, clocked Latch and flip flop circuits, CMOS D-latch and edge triggered flip flop - Basic principle, non ideal effects, domino CMOS Logic, high performance dynamic CMOS Circuits, Clocking Issues, Two phase clocking.

MODULE III CMOS SUB SYSTEM DESIGN 9

Data path circuits, Architectures for Adders Full adder circuit design, Inverting Adder, Carry Save Adder, Carry Select Adder, Carry Look Ahead Adder, Accumulators, Multipliers-Basic Terminology, Booth and Modified Booth Encoding, 2s Complement Arithmetic, Array Multiplier, Carry Save Multiplier, Signed multiplication and carry save implementation, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

MODULE IV INTERCONNECT &TIMING METRICS 9

Interconnect Parameters – Capacitance & Timing, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self Timed Circuit Design, Synchronizers and Arbiters, Clock Synthesis and Synchronization Using Phase-Locked Loop.

MODULE V DESIGNING MEMORY AND ARRAY STRUCTURES 8

SRAM and DRAM Memory Core - memory peripheral circuitry - Memory reliability and yield -Power dissipation in memories.

Total Hours 45

TEXT BOOK:

1. Jan M. Rabaey, AnanthaChadrakasan, BorivojeNikolic, “Digital Integrated Circuits: A Design Perspective”, Second Edition, PHI, 2016
2. Neil.H, E.Weste, David Harris, Ayan Banerjee, “CMOS VLSI Design: A Circuit and Systems Perspective”, Fourth Edition, Pearson Education, 2011.
3. Sorab K Gandhi, “VLSI Fabrication Principles: Si and GaAs”, Second Edition, John Wiley and Sons, 2010.

REFERENCE BOOK:

1. Sorab K Gandhi, “VLSI Fabrication Principles: Si and GaAs”, Second Edition, John Wiley and Sons, 2010.

OUTCOMES:

On completion of the course the student will be able to

- Demonstrate a clear understanding of CMOS fabrication flow and

technology scaling

- Design MOSFET based logic circuit
- Draw layout of a given logic circuit
- Realize logic circuits with different design styles
- Design CMOS circuits with different CMOS logic families
- Demonstrate an understanding of working principles of clocking, power reduction and distribution

ECD 6122	ADVANCED EMBEDDED SYSTEMS AND PROGRAMMING	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To explore Embedded system lifecycle
- To Introduce the occurrence of shared data problem and Interrupts in RTOS environment
- To familiarize the debugging in embedded systems.
- To learn Embedded C and Python programming.

PREREQUISITES

- Digital Electronics, Microprocessor and Microcontrollers

MODULE I EMBEDDED DESIGN 09

Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Interrupt routines in an RTOS environment –Hard Real Time scheduling considerations - Embedded platform bootsequence-power optimization techniques.

MODULE II MEMORY AND INTERFACING 09

Memory: Memory write ability and storage performance – Memory types –composing memory – Advance RAM interfacing - communication basic –Microprocessor interfacing I/O addressing – Interrupts – Direct memory access– Arbitration - Multilevel bus architecture.

MODULE III INTEGRATION AND TESTING OF EMBEDDED HARDWARE AND FIRMWARE 09

Integration of Hardware and Firmware - In system programming - The Integrated development environment-Debugging techniques- Host based debugging – Remote debugging – ROM emulators – Logic analyzer- Real time trace – Hardware break points – Overlay memory- Testing embedded software.

MODULE IV EMBEDDED C 09

Introduction to Embedded C - Difference between C & Embedded C - Programming style - Basic structure of C program- Keywords & Identifiers - Data type & its memory representation - Arrays and strings- Types of Operators - Bitwise Operators - Control Structures – Loops - Functions.

MODULE V PYTHON PROGRAMMING 09

Basics of PYTHON Programming Syntax and Style – Python Objects– Dictionaries – comparison with C programming on Conditionals and Loops – Files – Input and Output – Errors and Exceptions – Functions – Modules – Classes and OOP – Execution Environment.

Total Hours: : 45

TEXT BOOK:

1. Arnold S. Berger – "Embedded System Design: An introduction to processor,tools and techniques", CMP books, USA, 2002.
2. David. E. Simon, "An Embedded Software Primer", Pearson Education, 2001.
3. Peter Barry, Patrick Crowley, "Modern Embedded Computing" MorganKaufmann Publishers, 2012.

REFERENCE BOOK:

1. Michael J Pont, "Embedded C", Pearson Education, 2007.
2. Jivan S. Parab, Vinod G. Shelake, RajanishK.Kamot, and GourishM.Naik, "Exploring C for Microcontrollers- A Hands on Approach", Springer, 2007.
3. Mark Lutz, "Learning Python Powerful OOPs",O'reilly,2011.

OUTCOMES:

On completion of program students will be able to

- Analyze the quality principles and tools in embedded system during product development process
- Design energy efficient embedded systems
- Design interface circuit with processor and memory devices.
- Test and debug the coding in embedded systems
- Develop software programs to control embedded system using C and Python Languages.
- Generate product specification for embedded system

ECD 6123	CMOS MIXED SIGNAL CIRCUIT DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- Describe about the phase locked loop and applications
- Explain the digital to analog converting circuits and specifications
- knowledge on filter design in mixed signal mode
- Explain Analog to digital circuit and specification
- Explain filter circuit structure
- Investigate switched capacitor circuits

PREREQUISITES :

- Electronic circuits, VLSI design, Analog integrated circuit design

MODULE I DATA CONVERTER MODELLING 9

Sampling and Aliasing , The sample and Hold Impulse sampling,Spice model for DAC and ADC ,Ouantization noise ,Quantization noise –voltage spectral density-Data converter SNR –Improving SNR using averaging-Decimating filters for ADC-Interpolating filters for ADC –Bandpass and high pass sinc filters –Using feedback to improve SNR.

MODULE II NOISE SHAPING DATA CONVERTER 9

First order noise shaping –first order NS Modulators-RMS quantization noise in a first order modulator-Decimating and filtering the output of NS modulator-Analog implementation of first order NS modulator-Second order noise shaping-Noise shaping topologies-Higher order modulator-Multi bit modulator-Cascaded modulator-Bandpass modulators.

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MODULE III BAND PASS DATA CONVERTER & A HIGH-SPEED DATA CONVERTER 9

Continuous time band pass noise shaping-switched capacitor bandpass noise shaping- high speed converter topologies-Clocked signals –implementation and filtering-Generating clock signals in implementation

MODULE IV ADVANCED PHASE LOCKED LOOP 9

Basics of PLL, Analog PLL, Digital PLL,Wide tuning range PLL-Design issues with

wide tuning range PLL-PLL topology-ring oscillator-Frequency divider and phase frequency detector

MODULE V FILTERS 9

Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-C integrator, discrete time integrators. Filtering topologies - bilinear transfer function and bi-quadratic transfer function. Integrator-Based CMOS Filters: Integrator building blocks, filtering topologies, Filters using Noise-shaping.

Total Hours : 45

TEXT BOOKS:

1. Armin Tajalli, Yusuf Leblebici, Extreme Low-Power Mixed Signal IC Design: Subthreshold Source-Coupled Circuits, Springer, 2010
2. Jacob Baker, “CMOS Mixed-Signal circuit design”, IEEE Press, 2009.
3. Razavi, “Design of analog CMOS integrated circuits”, McGraw Hill, 2009.
4. Razavi, “Principles of data conversion system design”, S.Chand and company Ltd 2000

REFERENCE BOOKS:

1. Jacob Baker, CMOS: Circuit Design, Layout and Simulation, IEEE Press, 2009.
2. Gregorian, Temes, “Analog MOS Integrated Circuit for signal processing”,John Wiley & Sons, 1987.
3. Baker Li, Boyce, “CMOS: Circuit Design, layout and Simulation”, PHI, 2000.
4. Allen CMOS Analog Circuit Design Oxford University Press; Third edition 2013.
5. CMOS circuit design, layout and simulation by R. Jacob BakerRevised second edition, IEEE press, 2008.

ECD 6124	ADVANCED MICROCONTROLLER ARCHITECTURE AND PROGRAMMING	L	T	P	C
		3	0	2	4

OBJECTIVES:

- To know Microcontroller based system design, applications.
- To teach I/O interface in system Design
- To learn about Design and programming of MSP 430 microcontroller
- To study the ARM architecture and program
- To involve the students to Practice on Workbench /Software Tools/ Hardware Processor Boards with the supporting Peripherals

PREREQUISITES:

- Basics of microcontrollers, programming in assembly language

MODULE I 8051 MICROCONTROLLER ARCHITETURE 12

Architecture – memory organization – addressing modes – instruction set-I/O programming-Timer programming – Serial port programming-Interrupt programming

Laboratory Practice: Practice in 8051 microcontroller based assembly/C language programming-I/O programming -Timer Counter Programming – Serial Communication- practice in KEIL µvision IDE complier

MODULE II PIC MICROCONTROLLER ARCHITETURE 12

Architecture – memory organization – addressing modes –Overview instruction set - I/O ports-bank switching, I/O programming-Timer programming- ADC, DAC and Sensor interfacing, Practice in MPLAB compiler.

Laboratory Practice: Practice on PIC Microcontroller based Assembly/C language programming – Arithmetic Programming- practice in MPLAB compiler

MODULE III MSP430 ARCHITECTURE AND PROGRAMMING 12

Architecture – CPU features – Memory structure - Addressing modes – Instruction sets Interrupts programming– Input and Output programming– On-chip peripherals– Hardware considerations – Flash memory – Low power design-Practice in IAR workbench

Laboratory Practice: Practice on MSP430 Microcontroller based Assembly/C language I/O programming – Timer Counter Programming – Serial Communication-Programming Interrupt - practice in IAR workbench compiler.

MODULE IV ARM ARCHITECTURE AND PROGRAMMING 12

ARM Architecture-LPC2148- The ARM Programmer's model - Instruction set – Thumb instruction set – I/O Programming –UART programming- ADC-DAC-I2C programming-Bit manipulation and Bit Shifting –USB communication

Laboratory Practice: Embedded C -Port programming-Bit manipulation and shifting-UART programming –Practice in keil ARM.

MODULE V SYSTEM DESIGN – CASE STUDY 12

Interfacing LCD Display – Keypad Interfacing - Motor Control – Controlling DC/ AC appliances – Measurement of frequency - Stand-alone Data Acquisition System.

Laboratory Practice: Design a mini project using PIC or MSP430

Total Hours: 60

TEXT BOOKS:

1. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey "PIC Microcontroller and Embedded Systems using Assembly and C for PIC18", Pearson Education 2008
2. John Iovine, "PIC Microcontroller Project Book", McGraw Hill 2000
3. Rajkamal, "Microcontrollers Architecture, Programming",Interfacing&System Design",Pearson,2012

REFERENCES:

1. Chris Nagy, "Embedded systems design using the TI MSP430 series", Elsevier 2003.
2. Steve Furber, ARM System on Chip Architecture, Addison –Wesley Professional, 2014.

OUTCOMES:

On completion of the course the students will be able to

- Create ALP and C programs to develop applications using 8051 & PIC Microcontroller.
- Debugging the embedded programs under KEIL µvision and MPLAB IDE
- Describe the architecture of MSP series of microcontroller
- Create ALP and C programs to develop applications using the MSP430 Microcontroller
- Interface the internal and External IOs of PIC, MSP and ARM processor.
- Use KEIL µvision IDE,IAR Embedded workbench and MPLAB IDE.

ECD 6125	VLSI PHYSICAL DESIGN AUTOMATION LAB	L	T	P	C
		0	0	2	1

OBJECTIVES

- Make the students capable to design FPGA based digital systems
- Analyze the performance of the digital systems using EDA Tools
- Impart hands-on experience on the VLSI physical design tools.

PREREQUISITES:

- Basics of electronic circuit design, hands on experience in EDA tools

FPGA BASED EXPERIMENTS

1. Design of sequential and combinational circuits using verilog HDL
2. Data path and Controller architectures for combinational & sequential circuits using verilog HDL
3. Verilog examples for FPGA Implementation, I/O devices interfacing
4. Verilog examples illustrating Static and dynamic power Analysis-Xilinx ISE/Quartus
5. Verilog examples illustrating Static and dynamic Timing analysis procedures and constraints, Critical path considerations –. Xilinx ISE/Quartus
6. Designing FIR filter using Xilinx ISE System Generator and MATLAB simulink

ASIC BASED EXPERIMENTS

7. ASIC RTL realization using standard cell libraries- Cadence/Tanner/Mentor Graphics.
8. Static and dynamic power Analysis- Cadence/Tanner/Mentor Graphics.
9. Static and dynamic Timing analysis procedures and constraints.
10. Critical path considerations – Cadence/Tanner/Mentor Graphics.
11. Layout design, LVS, Back annotation- Cadence/TANNER/ Mentor Graphics

P:30 - Total Hours:30

OUTCOMES:

After successful completion of the course, the students will be able to

- Design digital circuits using verilog HDL
- Estimate and analyze the static and dynamic power of a digital system using EDA tools

- Estimate and analyze the timing performance of a digital system using EDA tools
- Develop digital systems meeting the functionality ,timing and power constraints using EDA tools
- Design layouts and schematic of digital circuit using EDA tools
- Work in projects involving the design of digital ICs

SEMESTER II

ECD 6201	RESEARCH METHODOLOGY FOR ENGINEERS	L	T	P	C
		3	1	0	4

OBJECTIVES:

- To provide a perspective on research to the scholars
- To educate on the research conceptions for designing the research
- To be trained about research, design, information retrieval, problem formulation.
- To impart knowledge on statistical techniques for hypothesis construction
- To gain knowledge on methods of data analysis and interpretation
- To learn about the effective communications of research finding and writing of research reports, papers and ethics in research.

PREREQUISITES :

- BASICS KNOWLEDGE OF ENGINEERING, PROBABILITY, STATISTICS

MODULE I RESEARCH PROBLEM FORMULATION 9

Research - Objectives - types, Research methods and methodology, Research process, solving engineering problems-Identification of research topic - Formulation of research problem, literature survey and review.

MODULE II RESEARCH DESIGN 10

Research design - meaning and need - basic concepts - Different research designs, Experimental design - principle - important experimental designs, Design of experimental setup, Mathematical modeling - Simulation, validation and experimentation - Dimensional analysis - similitude.

MODULE III Use Of Statistical Tools In Research 12

Importance of statistics in research - Concept of probability - Popular distributions - Sample design. Hypothesis testing, ANOVA, Design of experiments - Factorial designs - Orthogonal arrays.

MODULE IV : Data Collection, Analysis And Interpretation Of Data 10

Sources of Data, Use of Internet in Research, Types of Data - Research Data Processing and analysis - Interpretation of results- Correlation with scientific facts -

repeatability and reproducibility of results - Accuracy and precision –limitations, Application of Computer in Research- Spreadsheet tool, Presentation tool-Basic principles of Statistical Computation.

MODULE V Optimization Techniques 10

Use of optimization techniques - Traditional methods – Evolutionary Optimization Techniques. Multivariate analysis Techniques, Classifications, Characteristics, Applications -correlation and regression, Curve fitting.

MODULE VI The Research Report 9

Purpose of written report - Audience - Synopsis writing - preparing papers for International Journals, Software for paper formatting like LaTeX/MS Office, Reference Management Software, Software for detection of Plagiarism –Thesis writing, - Organization of contents - style of writing- graphs and charts - Referencing, Oral presentation and defence - Ethics in research - List of funding agencies in India - Methods of proposal submission - Patenting, Intellectual Property Rights.

Total Hours: 60

TEXT BOOKS

1. Ganesan R., Research Methodology for Engineers, MJP Publishers, Chennai, 2011.
2. Ernest O., Doebelin, Engineering Experimentation: planning, execution, reporting, McGraw Hill International edition, 1995.
3. George E. Dieter., Engineering Design, McGraw Hill – International edition, 2000.
4. Madhav S. Phadke, Quality Engineering using Robust Design, Printice Hall, Englewood Cliffs, New Jersey, 1989.
5. Kothari C.R., Research Methodology – Methods and Techniques, New Age International (P) Ltd, New Delhi, 2003.
6. Kalyanmoy Deb., “Genetic Algorithms for optimization”, KanGAL report, No.2001002.

REFERENCE BOOKS

1. Holeman, J.P., Experimental methods for Engineers, Tata McGraw Hill Publishing Co., Ltd., New Delhi, 2007.
2. Govt. of India, Intellectual Property Laws; Acts, Rules & Regulations, Universal Law Publishing Co. Pvt. Ltd., New Delhi 2010.

OUTCOMES:

At the end of the course, the student should be able to:

- Formulate the research problem
- Design and Analyze the research methodology
- Apply statistical techniques for hypothesis construction
- Construct and optimize the research hypothesis
- Analyze and interpret the data
- Report the research findings

ECD 6221 REAL TIME OPERATING SYSTEMS

L	T	P	C
3	0	0	3

OBJECTIVES:

The OBJECTIVES of the course is to

- Introduce the concepts of Operating systems and Real-time Operating Systems
- Impart knowledge on Resource management, time-constrained communication, scheduling and imprecise computations, real-time kernels and case studies.
- learn the kernel architecture of µC/OS-II RTOS
- Compare various RTOS

PREREQUISITES:

- Basics knowledge of Operating system, Embedded System

MODULE I REVIEW OF OPERATING SYSTEMS 09

Introduction- operating system services and structures-system calls- process management-process synchronization-classical synchronization problem-CPU scheduling.

MODULE II REAL TIME OPERATING SYSTEM AND SCHEDULING 09

Real-time System-Basic model-characteristics-safely,reliability-types-Timing constraints-Real time task scheduling-classification-clock driven-hybrid schedulers-Event driven scheduling –EDF –RMA-issues

MODULE III IPC in RTOS 09

Resource sharing –priority inversion-priority inheritance protocol-Highest Locker Protocol-Priority Ceiling Protocol-different types of priority inversions under PCP-Feature-issues in IPC protocol-Handling Task Dependencies

MODULE IV µC/OS-II RTOS 09

Introduction – Features-Kernel Structures- Task Management – Time Management-Event Control Block- Semaphores- Memory Management- Porting RTOS

MODULE V Commercial RTOS and application 09

Comparison and study of various RTOS –VRTX-QNX – VX works – RT Linux Case studies-RTOS for fault Tolerant Applications – RTOS for Control Systems.

L:45 - Total Hours:45

TEXT BOOKS:

1. Rajib Mall, Real-Time Systems: Theory and Practice, Pearson, 2009
2. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.
3. Jane W.S.Liu, Real Time Systems, Pearson Education, Asia, 2001.

REFERENCES:

1. Herma K., “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.
2. Charles Crowley, “Operating Systems-A Design Oriented approach” Tata McGraw Hill,1996

OUTCOMES:

After successful completion of the course, the students shall be able to

- Illustrate OS structure and explain process scheduling types.
- Compare the features of traditional OS and RTOS.
- Describe inter task communication and synchronization mechanisms.
- Analyze and design real time scheduling algorithms
- Select appropriate RTOS for the required application.
- Determine the common faults that occur in RTOS based embedded system.

ECD6222 ANALOG INTEGRATED CIRCUIT DESIGN

L	T	P	C
3	0	2	4

OBJECTIVES:

- Introduce the principles of analog circuits and apply the techniques for the design of analog integrated circuit
- Analysis, design, and applications of modern analog circuits using CMOS technologies.
- Analysis of basic Multipliers, wave shaping circuits and basic operation of PLL.
- Implement a complete analog system.

PREREQUISITES:

- Basics knowledge of Electronic Circuits, VLSI Design, CMOS technology

MODULE I INTRODUCTION 12

Analog MOS transistor models Temperature effects and Noise in MOS transistor MOS resistors, characterization of resistive, capacitive elements and MOS devices. Passive and active CMOS current sink/ sources. Effects due to nonlinearity and mismatch in MOS circuits.

Laboratory Practice

Verification of MOS Device Characterization and parametric (PAR) analysis, Current Mirrors: Simple, cascode, feedback and low-voltage

MODULE II SINGLE STAGE CMOS AMPLIFIERS 12

Basics of single stage CMOS amplifiers - common Source, common gate and source follower. Frequency response of common Source, common gate and source follower.

Laboratory Practice

Simulation of Single stage Amplifiers-Diode connected, Current Mirror Load, PMOS with self biased load and self biased CMOS.

MODULE III CMOS DIFFERENTIAL AMPLIFIERS 12

CMOS Operational Amplifiers- one stage and two stage OP-AMPS - Gain boosting- Common Feedback- Cascode and Folded cascade structures.

Laboratory Practice: Differential Amplifiers: Simple and cascode current mirrors.

MODULE IV HIGH PERFORMANCE OP-AMPS 12

High speed/ high frequency op-amps, micro power op-amps, low noise op-amps and low voltage op-amps. Current mirrors filter implementations. Supply independent and temperature independent references Band gap references PTAT current generation and constant Gm biasing – CMOS comparators – Multipliers and wave shaping circuits .

Laboratory Practice

Operational Trans-conductance Amplifiers (OTA), Two stage OP-AMP.

MODULE V SWITCHED CAPACITOR CIRCUITS 12

First and Second Order Switched Capacitor Circuits, Switched Capacitor filters, CMOS oscillators, simple and charge pump CMOS PLLs non ideal effects in PLLs, Delay locked loops, frequency locked loops and applications, basics of CMOS data converters – Medium and high speed CMOS data converters, Over sampling converters.

Laboratory Practice

Verification of switched capacitor Integrators.

Total Hours: 60

TEXT BOOKS:

1. David. A. Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley and Sons, 2016
2. BehzadRazavi, “Design of Analog CMOS Integrated Circuit”, Tata McGraw HILL, 2017.

REFERENCES:

1. Philip Allen & Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2013.
2. Mohammed Ismail &Feiz, “Analog VLSI – Signal Information and Processing”, John Wiley and Sons,1994.

OUTCOMES:

After successful completion of the course, the students shall be able to

- Characterize the MOSFET and perform parametric analysis for the simple MOS models.
- Analyze and design MOSFET based Amplifier circuits.
- Design and analyze band gap reference biasing sources.

- Design and analyze operational amplifier circuits
- Design and analyze switched capacitor based mixed signal circuits
- Use the Composer (schematic capture), Virtuoso (layout generation), Spectre HDL (circuit simulation), Diva tools (DRC, LVS, ERC, extraction) tools for designing analog integrated circuits.

ECD 6223 EMBEDDED SYSTEMS LABORATORY

L	T	P	C
0	0	2	1

OBJECTIVES:

- To gain knowledge in programming with software tools and microcontrollers with peripheral interfaces.
- To develop a program and simulate 32 bit microcontrollers in C programming.
- To learn programming with sensors
- To focus on the embedded system hardware development

PREREQUISITES:

- Basics knowledge of Embedded Systems

LIST OF EXPERIMENTS

DESIGN WITH 32 BIT MICROCONTROLLERS USING EMBEDDED C

1. ARM -LPC2148 Processor - I/O Programming.
2. ARM-LPC2148 -Serial communication programming –RS232
3. ARM -LPC2148 Processor-ADC/DAC programming.
4. ARM-Cortex M3-LPC1768 –LCD /Graphical LCD interfacing, Stepper motor
5. ARM-Cortex M3-LPC1768 –CAN programming
6. Multitasking in RTOS
7. Scheduling in any one type of Real Time Operating Systems (RTOS)`

PROGRAMMING SoC USING PYTHON LANGUAGE

8. Sensor interfacing with SoC
9. Camera interfacing with Soc
10. GUI design using python
11. Mini-project

P:30 - Total Hours:30

OUTCOMES:

On completion of program students will be able to

- Simulate simple application programs through Keil µ vision.
- Interface I/O ports, timers, seven segments LED, serial ports with ARM Microcontrollers.
- Demonstrate programming with CAN controller
- Implement Multitasking and Scheduling in RTOS Environment
- Identify new developments in SOC and programming
- Program in SoC using Python Language

VALUE ADDED COURSE	L	T	P	C
	0	0	0	0

OBJECTIVES:

- To expose the latest technology / tools used in the industry and enable the students acquire knowledge and skill set in the same.

GENERAL GUIDELINES:

- Students should undergo any relevant certification course offered by the institution or other institutions / universities / IIT / IISc etc. for a minimum of 40 hours.
- Selection and completion of value added course by the students shall be endorsed by Head of the Department.

OUTCOMES:

- Students should be exposed and gained knowledge in any one latest technology used in the industry

SEMESTER III

ECD 7121	PROJECT WORK – PHASE I	L	T	P	C
		0	0	12	6

OBJECTIVES:

- To improve the professional competency and research aptitude
- Aims to develop the work practice of students to apply theoretical and practical tools/techniques
- To solve real life problems related to industry and current research
- To improve the skills towards report/documentation preparation

GUIDELINES:

Project work can be a design project/experimental project and/or computer simulation project on any of the topics of communication systems. The project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential (Industry oriented Projects), they may be permitted to continue their project outside the parent institute. Department will constitute an Evaluation Committee to review the project work. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.

The student is required to undertake the master research project phase 1 during the third semester and the same is continued in the 4thsemester (Phase 2). Phase 1 consist of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review would highlight the topic, Objectives, methodology and expected results. Second review evaluates the progress of the work, preliminary report and scope of the work which is to be completed in the 4th semester. The Evaluation committee consists of at least four faculty members of which internal guide and other experts in the specified area of the project shall be two essential members.

OUTCOMES:

At the end of the project work phase I the student will be able to

- learn the tool required for the design, analysis of their preliminary work
- Select the specific devices for different application along with justification
- Apply the practical knowledge while solving real time problems
- Incorporate cost effective and efficient project models
- Conclude the subject knowledge through proto type models
- Prepare an appropriate documentation

ECD 7122	INTERNSHIP	L	T	P	C
		0	0	3	1

OBJECTIVES:

- To improve the professional competency, Industrial Exposure and research aptitude of students
- To develop the work practice through design skills inside the industry for solving real life problems

GUIDELINES:

1. This internship to be carried out in the industry for solving real life problems.
2. The internship is a core industry type of training to build an experimental/prototype project on any of the topics in electronics and communication.
3. Department will constitute an Evaluation Committee to review the internship periodically including the industry expert.
4. The Evaluation committee consists of at least three faculty members of which internal guide and another two experts in the specified area of the project.

OUTCOMES:

At the end of the internship the student will be able to

- Design and analyze an electronic and communication system
- Select or utilize the appropriate component\technology to solve the given problem
- Fabricate an electronic system/device in their area of interest
- Demonstrate the working module
- Improve their presentation skills
- Improve the documentation skills

MOOC COURSE	L	T	P	C
	0	0	0	0

OBJECTIVES:

- To learn the basics principles and concepts of the topic in which a project work is undertaken by the student.

GENERAL GUIDELINES:

- Students shall identify a MOOC course related to his/her project topic in consultation with the project supervisor.
- Student shall register for a MOOC course with minimum two credit offered by any recognized organization during the project phase I.
- Selection and completion of MOOC course by the students shall be endorsed by Head of the Department.

OUTCOMES:

Students will be able to

- Familiarize the basic principles and concepts related to the topic of his/her project work.
- Utilize the knowledge gained in the field of study to perform literature review with ease.
- Formulate the experimental / analytical methodology required for the project work

SEMESTER IV

ECD 7121	PROJECT WORK – PHASE II	L	T	P	C
		0	0	36	18

OBJECTIVES:

- To improve the professional competency and research aptitude
- Aims to develop the work practice of students to apply theoretical and practical tools/techniques
- To solve real life problems related to industry and current research
- To improve the skills towards report/documentation preparation

GUIDELINES:

Project work can be a design project/experimental project and/or computer simulation project on any of the topics of communication systems. The project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential (Industry oriented Projects), they may be permitted to continue their project outside the parent institute. Department will constitute an Evaluation Committee to review the project work. The Evaluation committee consists of at least three faculty members of which internal guide and another two experts in the specified area of the project.

The student is required to undertake the master research project phase 1 during the third semester and the same is continued in the 4thsemester (Phase 2). Phase 1 consist of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review would highlight the topic, Objectives, methodology and expected results. Second review evaluates the progress of the work, preliminary report and scope of the work which is to be completed in the 4th semester. The Evaluation committee consists of at least four faculty members of which internal guide and other experts in the specified area of the project shall be two essential members.

OUTCOMES:

At the end of the project work phase I the student will be able to

- learn the tool required for the design, analysis of their preliminary work
- Select the specific devices for different application along with justification
- Apply the practical knowledge while solving real time problems
- Incorporate cost effective and efficient project models
- Conclude the subject knowledge through proto type models
- Prepare an appropriate documentation\Report

PROFESSIONAL ELECTIVES- VLSI

ECDY051	CAD FOR VLSI CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To impart knowledge on fundamentals of CAD tools for the modelling, design, analysis, test, and verification of digital VLSI systems
- To study various layout design methods in VLSI
- To know the different partitioning algorithms in VLSI design
- To understand the concepts behind the floor planning techniques
- To use the types of routing methods
- To learn about the hardware models for higher level synthesis

PREREQUISITES :

- Basic knowledge in Digital CMOS systems and data structure algorithms.

MODULE I VLSI DESIGN FLOW 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity- Tractable and Intractable problems - General purpose methods for combinatorial optimization.

MODULE II LAYOUT AND PARTITIONING 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - Partitioning Algorithms - Group Migration Algorithm, Simulated Annealing and Evolution, Other Partitioning Algorithms - Performance Driven Partitioning.

MODULE III PLACEMENT 9

Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement, Over-the-Cell Routing, Via Minimisation, Clock Routing, Power and Ground Routing.

MODULE IV FLOOR PLANNING AND ROUTING 9

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

MODULE V HIGH LEVEL SYNTHESIS 9

Study of Hardware models for high level synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem.

TOTAL HOURS: 45

TEXT BOOKS:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley & Sons, 2002.
2. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Springer International Edition, 2005.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOK:

1. Erik Brunvand, Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Pearson, 2010.
2. Samir Palnitkar, Verilog HDL, Second Edition, Pearson Education, 2004.

OUTCOMES :

On completion of the course the student will be able to

- Demonstrate the knowledge of CAD tools for the design of digital VLSI circuits.
- Discuss the physical layout design rules
- Describe the problems optimization algorithms in placement and partitioning.
- Illustrate the Floor planning concepts and its representation.
- Analyse the various optimization algorithms in VLSI Routing
- Develop hardware models and synthesis algorithms for VLSI CAD tools

ECDY052	ASIC DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To know the design flow of different types of ASIC
- To familiarize the different types of programming technologies and logic devices
- To disseminate various programmable ASIC architecture
- To impart knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC
- To analyze the synthesis, Simulation and testing of systems
- To learn the different high performance algorithms and its applications in ASIC

PREREQUISITES :

- To know about the basic concepts of Digital circuit design and hardware programming language.

MODULE I INTRODUCTION TO ASICs AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors, CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort – Library cell design.

MODULE II PROGRAMMABLE ASICs AND LOGIC CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

MODULE III PROGRAMMABLE ASIC INTERCONNECTS AND LOW LEVEL DESIGN LANGUAGES 9

Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 –Design systems - Logic Synthesis - Half gate ASIC - Schematic entry - Low level design language .

MODULE IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

MODULE V ASIC PHYSICAL DESIGN 9

System partition -partitioning – partitioning methods – interconnect delay models and measurement of delay – floor planning – placement – Routing: global routing – detailed routing – special routing – circuit extraction – DRC

Total Hours : 45

TEXT BOOKS:

1. M.J.S .Smith, "Application Specific Integrated Circuits ", Addison -Wesley Longman Inc., 2003.
2. H.Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1999
3. H. Bhatnagar, “Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime”, 2nd edition, 2001.

REFERENCES:

1. Keith Barr “ASIC Design in the Silicon Sandbox: A Complete Guide to Building Mixed-Signal Integrated Circuits”, McGrawHill, 2006.
2. Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996.
3. J.M.Rabaey, A. Chandrakasan and B.Nikolic, Digital Integrated Circuit Design Perspective (2/e), PHI 2003.
4. D. A.Hodges, Analysis and Design of Digital Integrated Circuits (3/e), MGH 2004.

OUTCOMES :

On completion of the course the student will be able to

- Explain the ASIC Design Flow and ASIC library design
- Program logic device using different programming technologies
- Illustrate the various programmable ASIC structure with its logic cells
- Describe the Logic Synthesis and Testing methodologies
- Identify, test and rectify faults in I/O cells and interconnects
- Demonstrate and solve the complexity in physical design of ASIC using optimized algorithms

ECDY053 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To provide knowledge to design synchronous sequential circuit.
- To provide knowledge to design asynchronous sequential circuit.
- To introduce programmable logic devices.
- To Analyze digital system design using PLD.
- To introduce the concepts involved in designing fault free circuits.
- To implement digital systems using VERILOG.

PREREQUISITES:

- Basic knowledge on digital electronics , memory devices & Verilog

MODULE I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN– State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits, Design of Arithmetic circuits for Fast adder- Array Multiplier.

MODULE II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Asynchronous sequential circuit design, Derivation of excitation table, Designing with SM charts – State machine charts, Derivation of SM charts, and Realization of SM charts-Hazards- Designing railway ticket vending Machine Controller.

MODULE III DESIGNING WITH PROGRAMMABLE LOGIC DEVICES 9

Read-Only Memory, Read/Write Memory, Static RAM, Dynamic RAM, Complex Programmable Logic Devices, Field-Programmable Gate Arrays-Realization State machine using PLD Designing a synchronous sequential circuit using PLA/PAL.

MODULE IV FAULT DIAGONOSIS AND TESTING 9

Fault detection and location, gate sensitivity, path sensitization, undetectable faults, bridging fault, two level circuit fault detection, Boolean difference –D algorithm - Tolerance techniques, compact testing technique; scan path testing, design for testability.

MODULE V SYSTEM DESIGN USING VERILOG 9

Hardware Modeling with Verilog HDL – Logic System, Data Types and Operators For Modeling in Verilog HDL - Behavioral Descriptions in Verilog HDL – HDL based Synthesis – Synthesis of Finite State Machines– structural modeling –compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider –Verilog design of programmable logic devices- Design of simple microprocessor.

Total Hours: 45

TEXT BOOKS:

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill, 2002.”, Pearson , 2003.
2. Stephen Brown and ZvonkVranesic, “Fundamentals of Digital Logic with Verilog Design”, Tata McGraw Hill, 2002.
3. Parag K Lala, “Digital System design using PLD”, BS Publications, 2003.

REFERENCES

1. Lizy Kurian John , Charles H. Roth Digital System Design Using VHDL Thomson Press (India) Ltd, 2012
2. M.D.Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, Prentice Hall, 1999
3. Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, Prentice Hall PTR, Second Edition 2003

OUTCOMES:

On completion of the course, students will be able to

- To analyze clocked synchronous sequential circuits and design digital systems based on the given specifications.
- To analyze asynchronous sequential circuits and design digital systems based on the given specifications
- To make state machines and ASM charts for the given design requirements.
- To select and use appropriate PLDs to realize digital systems based on the requirements.
- To perform fault diagnosis and testing in digital circuit
- To apply the digital system design principles and make projects based on the requirements.

ECDY 054 MEMS SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

- Provide the basic of MEMS
- Understand the basic of design constraints and the factors like stress, strain and etc.
- Know the basic of Electrostatic design
- Introduce the concepts of MEMS Electronic Sensors, Optical and RF system
- Analyze circuit and system issues
- Create MEMS based device

PREREQUISITES :

- Basics operation of electronics Devices, Sensors, Optical and RF devices.

MODULE I INTRODUCTION TO MEMS 9

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication.

MODULE II MECHANICS FOR MEMS DESIGN 9

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics - actuators, force and response time, Fracture and thin film mechanics.

MODULE III ELECTROSTATIC DESIGN 9

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators

MODULE IV CIRCUIT AND SYSTEM ISSUES 9

Electronic Interfaces, Feedback systems, Noise , Circuit and system issues, Case studies - Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

MODULE V INTRODUCTION TO OPTICAL AND RF MEMS 9

Optical MEMS - System design basics - Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF MEMS - design basics, case study - Capacitive RF MEMS switch, performance issues.

Total Hours: 45

TEXT BOOKS:

1. Stephen Santuria," Microsystems Design", Springer Science & Business Media, 08-May-2007
2. NadimMaluf," An introduction to Micro electromechanical system design", Artech House, 2004.
3. Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton, 2001.

REFERENCE BOOKS:

1. R. Ghodssi and P. Lin , “MEMS materials and processes handbook”, Springer 2011.
2. Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

OUTCOMES :

On completion of the course the student will be able to

- Describe the process of MEMS fabrication
- Describe the mechanisms followed to design MEMS devices
- Elucidate the methods to make electrostatic MEMS sensors
- Elucidate the methods to make MEMS based accelerometers
- Describe the MEMS based RF Switches
- Discuss the MEMS based optical scanners and sensors

ECDY 055 OPTIMIZATION TECHNIQUES AND THEIR APPLICATIONS IN VLSI DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

- To introduce the concepts of statistical modeling and test generation patterns
- To describe and analyze placement and power estimation
- To discuss about various convex optimization techniques
- To gain knowledge in fundamentals of genetic algorithms
- To provide overview of encoding in genetic algorithms
- To acquire knowledge on genetic algorithm routing procedures

PREREQUISITES :

- Basic knowledge about VLSI design.

MODULE I STATISTICAL MODELING 08

Modeling sources of variations- Monte Carlo techniques- Process variation modeling- Pelgrom's model, Principal component based modeling, Quad tree based modeling-Performance modeling-Response surface methodology, delay modeling, interconnect delay models

MODULE II STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS 08

Statistical timing analysis-parameter space techniques- Bayesian networks - Leakage models -High level statistical analysis- Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation - gate level yield estimation.

MODULE III CONVEX OPTIMIZATION 09

Convex sets -convex functions- geometric programming, trade-off and sensitivity analysis -Generalized geometric programming, geometric programming applied to digital circuit gate sizing-Floor planning -wire sizing -Approximation and fitting-Monomial fitting, Max- monomial fitting, Posynomial fitting.

MODULE IV GENETIC ALGORITHM AND ENCODING 11

Introduction, GA Terminology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic Placement, Routing -Technologymapping for FPGAs- Automatic test generation-Partitioning algorithm Taxonomy-Multiway Partitioning -Hybrid genetic-encoding-local improvement-Weighted DFS Reordering(WDFR)-Comparison of GAs-Standard cell placement-GASP algorithm-unified algorithm

MODULE V GA ROUTING PROCEDURES AND POWER ESTIMATION 09

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures. Power estimation-application of GA-Standard cell placement-GA for Automatic Test Generation.

Total Hours: 45

TEXT BOOKS

1. AshishSrivastava, Dennis Sylvester, David Blaauw “Statistical Analysis and Optimization for VLSI:Timing and Power”, Springer, 2006.
2. Andrew B. Kahng, Jens Lienig, Igor L. Markov, “VLSI Physical Design: From Graph Partitioning to Timing Closure”,Springer science ,2011
3. Stephen Boyd, “Convex Optimization”, Cambridge University Press, Second Edition, 2016.

REFERENCE BOOKS

1. Stephen Boyd, LievenVandenberghe “Convex Optimization”, Cambridge University Press, 2004.
2. PinakiMazumder, E.Mrudnick, “Genetic Algorithm for VLSI Design, Layout and test Automation”, Prentice Hall,1998

OUTCOMES :

On completion of the course the student will be able to

- Explain the basic optimization techniques
- Select and implement appropriate formulations and algorithms.
- Develop the capability to analyze on various statistical methods in analyzing a sample
- Analyze the concepts of genetic algorithms and genetic encoding.
- Appiy genetic algorithms for power estimation.
- Describe the genetic algorithm routing procedures

ECDY 056 PROGRAMMING VERILOG HDL

L	T	P	C
3	0	2	4

OBJECTIVES:

The primary course Objectives is to

- Learn the hardware description language Verilog HDL.
- Learn the hardware description language Verilog AMS
- Design of analog circuits using verilog AMS.
- Create and verify systems implemented using PLDs
- Design of single cycle CPU design.

PREREQUISITES :

- VLSI Design

MODULE I VERILOG HDL INTRODUCTION 06+06

Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Language Constructs and Conventions, Data Types, Scalars and Vectors, Parameters, Operators, Gate level Modeling , Dataflow Modeling, Behaviour modeling , Structural modelling ,Task and Functions.

Laboratory Practice Simulation of Verilog HDL programs illustrating the language constructs in the module I

MODULE II COMBINATIONAL LOGIC CIRCUITS USING VERILOG HDL 06+06

Design of Boolean expressions-Logic equations-Multiplexers-comparator-Programmable read only memories-Programmable array logic-Programmable logic array.

Laboratory Practice: Simulation of Verilog HDL programs illustrating the language constructs in the module II

MODULE III SEQUENTIAL LOGIC DESIGN USING VERILOG HDL 06+06

Design of synchronous sequential machines-synthesis procedure-equivalent states-Melay machines- Synchronous register and counters- Design of Asynchronous sequential machines-hazards-oscillations –races –Design of pulse mode asynchronous sequential machines.

Lab Practice: Verilog HDL programs illustrating the language constructs in the module III

MODULE IV ANALOG MODELLING USING VERILOG AMS 06+06

Modeling of resistors,capacitor,inductor,voltage and current sources-junction diode-resistive poer-delay-Voltage controlled oscillator-Sampling and hold circuits-Time interval measurement-Analog to digital converter-Digital to analog converter-Tolerence

Laboratory Practice: Simulation of Verilog AMS HDL programs illustrating the language constructs in the module IV

MODULE V SINGLE CYCLE CPU DESIGN IN VERILOG HDL 06+06

Circuits required for executing an instruction-Register file design-single cycle CPU data path design-Single cycle CPU control unit design-test program and simulations.

Laboratory Practice: Simulation of Verilog AMS HDL programs illustrating the language constructs in the module V

Total Hours : 60

TEXT BOOK :

1. Joseph Cavanagh , Verilog HDL Design Examples,CRC press 2018.
2. Yamin Li, Tsinghua Computer Principles and Design in Verilog HDL ,Wiley , Tsinghua University Press 2015
3. ZainalabdienNavabi, Verliog Digital System Design,TMH, 2nd Edition.

REFERENCES :

1. Fundamentals of Digital Logic with Verilog Design - Stephen Brown, ZvonkocVranesic, TMH, 2nd Edition,2007
2. Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
3. Advanced Digital Design with Verilog HDL - Michel D. Ciletti, PHI, 2009.
4. Kenneth S Kundert, Olaf Zinke, Designers Guide to Verilog AMS, Springer, 2004

OUTCOMES :

On completion of the course the student will be able to

- To Differentiate sequential language and concurrent language
- To Design and verify combinational logic circuits using Verilog HDL Design
- To verify sequential logic circuits using Verilog HDL
- To Implement programmable logic devices.
- Design analog circuits using verilog AMS
- Work as a HDL programmer

ECDY 057	RECONFIGURABLE COMPUTING	L	T	P	C
		3	0	0	3

OBJECTIVES:

The OBJECTIVES of the course is

- To investigate the state-of-the-art in reconfigurable computing both from a hardware and software perspective.
- To make the students understand both how to architect a reconfigurable systems and how to apply them for solving challenging computational problems.
- To examine specific contemporary reconfigurable computing systems and to identify existing system limitations and to highlight opportunities for research in dynamic and partial configuration areas.
- To impart knowledge on the application development of reconfigurable systems.

PREREQUISITES :

- VLSI Design

MODULE I INTRODUCTION 09

Introduction, origin of reconfigurable computing, Reconfigurable computing architecture, Reconfigurable computing hardware, Logic—The Computational Fabric, The Array and Interconnect, Extending Logic, Configuration, Case Studies, Altera Stratix, Xilinx Virtex-II Pro.

MODULE II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS 09

Reconfigurable Processing Fabric Architectures, RPF Integration into Traditional Computing Systems, Reconfigurable computing systems, Early Systems, PAM, VCC, and Splash , Small-scale Reconfigurable Systems, Circuit Emulation, Accelerating Technology, Reconfigurable Supercomputing, Other System Issues, The Future of Reconfigurable Systems

MODULE III PROGRAMMING RECONFIGURABLE SYSTEMS, COMPUTATION MODELS AND SYSTEM ARCHITECTURES 09

Computation Models Challenges, Common Primitives, Dataflow, Sequential Control, Data Parallel, Data-centric , Multi-threaded, Other Compute Models,

System Architectures - Streaming Dataflow, Sequential Control, Bulk Synchronous Parallelism, Data Parallel, Cellular Automata, Multi-threaded, Hierarchical Composition.

MODULE IV FPGA DESIGN 09

FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

MODULE V APPLICATION DEVELOPMENT 09

Implementing Applications with FPGAs, Strengths and Weaknesses of FPGAs, Application Characteristics and Performance, General Implementation Strategies for FPGA-based Systems, Implementing Arithmetic in FPGAs, Hardware/Software Partitioning.

Total Hours : 45

TEXT BOOK

1. Scott Hauck, André DeHon, “Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation”, Morgan Kauffman publishers, 2010.
2. M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2010.
3. C. Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer, 2010.

REFERENCES:

1. P. Lysaght and W. Rosenstiel, “New Algorithms, Architectures and Applications for Reconfigurable Computing”, Springer, 2005.
2. W. Wolf, “FPGA Based System Design”, Prentice-Hall, 2004.

OUTCOMES :

On completion of the course the student will be able to

- Describe various Reconfigurable Computing architectures systems
- Summarize the Programming model for Reconfigurable computing
- Design reconfigurable computing architectures on FPGA
- Apply Reconfigurable computing for hardware and software partitioning.
- Design and build an SOPC for a specific application.
- Develop arithmetic and complex digital architectures on FPGA

ECDY 058 RF INTEGRATED CIRCUITS DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

The OBJECTIVES of the course is

- To impart knowledge on LNA, Power amplifiers, PLL, Oscillators and frequency synthesizers
- To know the methods of designing passive components in IC.
- To discuss the importance of impedance matching techniques,
- To understand the transreceiver architectures.
- To know the effect of noise in RF.
- To introduce the design of the basic building blocks of RFIC.

PREREQUISITES :

- Semiconductor devices, Analog Circuits, Analog IC Design.

MODULE I IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs. MOSFET amplifier controlled by AGC.

MODULE II FEEDBACK SYSTEMS AND POWER AMPLIFIERS 8

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

MODULE III PLL AND FREQUENCY SYNTHESIZERS 8

Linearized Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer- N frequency synthesizers, Direct Digital Frequency synthesizers.

MODULE IV MIXERS AND OSCILLATORS 8

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators, Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

MODULE V NOISE AND TRANSCEIVER ARCHITECTURES 12

Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures upconversion Transmitter ,GSM radio architectures, CDMA, UMTS radio architectures.

Total Hours: 45

TEXT BOOK

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004, Reprint 2009.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 2e, 2013.

REFERENCES

1. Jan Crols, MichielSteyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
2. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2e, 2017

OUTCOMES :

On completion of the course the student will be able to

- Describe and select appropriate RF transceiver architectures based on the requirements.
- Describe the different topologies used to design passive components in IC
- Analyze Low Noise and power amplifier circuits and design the same based on the given requirements.
- Describe and analyze the performance of frequency synthesizers
- Analyze mixers and oscillator circuits and design the same based on the given requirements.
- Design the building blocks of RF transceiver system

ECDY 059 SEMICONDUCTOR MEMORIES

L	T	P	C
3	0	0	3

OBJECTIVES:

The OBJECTIVES of the course is

- To study the concepts of random-access memory.
- To study the concepts of Dynamic Random - access memories.
- To learn about nonvolatile memories.
- To learn the implementation methods in designing and making semiconductor memories
- To understand the problems involved in implementation of memories
- To understand different fault modeling and testing techniques

PREREQUISITES :

- Basics of digital memory

MODULE I STATIC RANDOM ACCESS MEMORY TECHNOLOGY 9

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAM.

MODULE II DYNAMIC RANDOM ACCESS MEMORY TECHNOLOGY 9

Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures -BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs

MODULE III NON VOLATILE MEMORIES 9

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS, PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture- Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

MODULE IV FAULT MODELING AND TESTING 9

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

MODULE V RELIABILITY AND RADIATION EFFECTS 9

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modeling, Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

Total Hours : 45

TEXT BOOKS:

1. Ashok K.Sharma, "Semiconductor Memories Technology, Testing and Reliability", Wiley, 10-Sep-2002 - Technology & Engineering
2. TegzeP.Haraszti, “CMOS Memory Circuits”, Springer Science & Business Media, 08-May-2007.

REFERENCES

1. Betty Prince,“Emerging Memories: Technologies and Trends”, Springer Science & Business Media, 08-May-2007

OUTCOMES :

On completion of the course the student will be able to

- Discuss the advancements in the SRAM and DRAM based memory technologies
- Analyze and interpret the design parameters used to design memory cells
- Describe the advancements in non-volatile memory design techniques
- Use fault modeling techniques to test memories
- Select appropriate technique to test memory devices
- To use suitable memory devices based on the requirements

ECDY 060 SoC DESIGN AND VERIFICATION

L	T	P	C
3	0	0	3

OBJECTIVES:

The OBJECTIVES of the course is

- Know the System on Chip with its need, Combinational logic and power optimization.
- Describe how the SoCs are designed in industrial environment using different design methodologies
- Examine the on chip components interconnected in a SoC.
- Analyze and solve problems in traditional bus based communication architecture using network on chip.

PREREQUISITES :

- Basics of VLSI Design

MODULE I INTRODUCTION TO LOGIC GATES & COMBINATIONAL LOGIC NETWORKS **9**

Introduction to logic gates & combinational logic networks, Combinational Logic Functions, Combinational Network Delay. Logic and interconnect Design. Power Optimization

MODULE II SYSTEM ON CHIP DESIGN PROCESS **9**

A canonical SoC Design, SoC Design flow waterfall vs spiral, top down vs Bottom up. Specification requirement, Types of Specification , System Design process, System level design issues, Soft IP Vs Hard IP, Design for timing closure, Logic design issues, Verification strategy, On Chip Buses.

MODULE III MACRO DESIGN PROCESS **9**

Top level Macro Design, Macro Integration, Soft Macro productization, Developing hard macros, Design issues for hard macros, Design, System Integration with reusable macros.

MODULE IV SoC VERIFICATION **9**

Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co-verification and Static net list verification.

Verification architecture, Verification components, Introduction to VMM, OVM and UVM.

MODULE V DESIGN OF COMMUNICATION ARCHITECTURES FOR SoCS **9**

On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures, Communication architecture tuners, Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification.

Total Hours : 45

TEXT BOOKS:

1. PrakashRashinkar Peter Paterson and Leena Singh “SoC Verification Methodology and Techniques”, Kluwer Academic Publishers, 2002.
2. Michael Keating, Pierre Bricaud, “Reuse Methodology manual for System on A Chip Designs”, Kluwer Academic Publishers, second edition, 2001.
3. William K. Lam, “Design Verification: Simulation and Formal Method based Approaches”, Prentice Hall. 2005.

REFERENCE BOOKS:

1. RochitRajsuman, “System- on -a- Chip Design and Test”, ISBN,2000
2. A.A. Jerraya, W.Wolf “Multiprocessor Systemsonchips”, M K Publishers,2004
3. Dirk Jansen “The EDA HandBook”, Kluwer Academic Publishers,2010

OUTCOMES :

On completion of the course the student will be able to

- Analyze CMOS VLSI Technologies along with performance parameters
- Describe the top-down and bottom-up design flows, timing problems.
- Design and implement data path elements such as ALUs, Multipliers.
- Investigate various power optimization and timing issues related to complex digital systems
- Use techniques for designing MPSoC and its performance.
- Illustrate the bus architectures of NOCs and routing.

ECDY 061 TESTING OF VLSI CIRCUITS

L	T	P	C
3	0	0	3

OBJECTIVES:

The OBJECTIVES of the course is

- Automated and manual techniques for generating tests for faults in digital circuits and systems.
- Generation of test vectors for combinational and sequential circuits
- Generation of built in self test patterns
- Crosstalk faults effects and test pattern generation
- Knowledge on Testing of algorithms for digital circuits.
- To learn various testing methods for digital circuits.

PREREQUISITES :

- Advanced digital system design, Digital system design.

MODULE I FAULTS IN LOGIC CIRCUITS AND TEST GENERATION 9

Faults in Logic Circuits-Stuck-at Fault- Bridging Faults- Delay Fault -Breaks and Transistors Stuck-Open and Stuck-On or Stuck-Open Faults in CMOS-Stuck-on and Stuck-Open Faults.

Test Generation for Combinational Logic Circuits-Truth Table and Fault Matrix-Path Sensitization- D-Algorithm -PODEM –FAN-Delay Fault Detection -Testing of Sequential Circuits -Designing Checking Experiments-Test Generation Using the Circuit Structure and the State Table.

MODULE II DESIGN FOR TESTABILITY 9

Design for Testability -Ad Hoc Techniques-Scan-Path Technique for Testable Sequential Circuit Design - Level-Sensitive Scan Design -Clocked Hazard-Free Latches -Double-Latch and Single-Latch LSSD -Random Access Scan Technique - Partial Scan-Testable Sequential Circuit Design Using Nonscan Techniques-Crosscheck-Boundary Scan.

MODULE III BUILT-IN SELF-TEST 9

Built-in Self-Test -Test Pattern Generation for BIST-Exhaustive Testing – Pseudo exhaustive Pattern Generation -Pseudorandom Pattern Generator- Deterministic Testing -Output Response Analysis -Transition Count- Syndrome Checking -

Signature Analysis -BIST Architectures -Built-in Logic Block Observer-Self-Testing Using an MISR and Parallel Shift Register Sequence Generator -LSSD on-Chip Self-Test .

MODULE IV TEST APPLICATION SCHEMES FOR TESTING DELAY EFFECTS AND DELAY MODELS 9

Enhanced scan test-standard scan test-slow_fast_slow clock test-At speed testing-Delay fault models-transition fault model-Gate delay fault model-Line delay fault model-path delay fault model-Segment delay fault model.

MODULE V TEST GENERATION ALGORITHMS FOR CROSS TALK FAULTS IN VLSI CIRCUITS 9

Test generation algorithms-Test genearation for crosstalk pulses-Deterministic algorithm-simulation based TG-Test generation technique for cross talk delay faults-Delay testing of asynchronous sequential circuits.

Total Hours : 45

TEXT BOOKS:

1. An Introduction to Logic Circuit Testing Parag K. Lala Texas A&M University–Texarkana,2009
2. Delay fault testing for VLSI circuits-Angela kristic,Springer science 2013.
3. S.Jayanthy, MC Bhuvaneshwari,Test generation of cross talk delay faults in VLSI circuits,Springer 2019.

REFERENCES:

1. Bushnell and Agrawal,Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits,Kluwer Academic Publishers, 2000
2. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.

OUTCOMES:

On completion of the course the student will be able to

- Generate test vectors using stuck at models for combinational circuits
- Design circuit with testability perspective
- Design test vector for sequential circuits
- Describe the architecture of built in self test and fault diagnosis.
- Discuss the delay fault test generation
- Design the test pattern for cross talk fault

ECDY 062 VLSI DIGITAL SIGNAL PROCESSING

L	T	P	C
3	0	0	3

OBJECTIVES:

The OBJECTIVES of the course is

- Introduce students to the fundamentals of VLSI signal processing and expose them to examples of applications.
- Design and optimize VLSI architectures for basic DSP algorithms.
- Understand the VLSI design models various domains of signal processing
- Develop the architectures for arithmetic operations
- Understand the noise effects in vlsi signal processing
- Design of systems using VLSI Cordic processing technique.

PREREQUISITES :

- VLSI signal processing (UG course),DSP

MODULE I BASICS VLSI SIGNAL PROCESSING ARCHITECTURE 10

Pipe lining and parallel processing for signal processing. Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining .Retiming- Solving System of Inequalities, Retiming Techniques.
Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.

MODULE II VLSI SPATIAL SIGNAL PROCESSING 7

General VLSI signal processing model-Frequency domain signal processing-Time domain signal processing and spatial domain signal processing-VLSI spatial noise effects-Coorelative double signalling-Symmetry VLSI signal processing.

MODULE III SYSTOLIC ARCHITECTURE AND FAST CONVOLUTION DESIGN. 8

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays-Fast Convolution: Introduction, Cook, Toom Algorithm, Winogard

Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

MODULE IV SHIFT-ADD CIRCUITS FOR CONSTANT MULTIPLICATIONS 10

Representation of Constants - Single Constant Multiplication - Direct Simplification from a Given Number Representation -Simplification by Redundant Signed Digit Representation-Simplification by Adder Graph Approach -State of the Art in SCM - Algorithms for Multiple Constant Multiplications -MCM for FIR Digital Filter and Basic Considerations -The Adder Graph Approach - Common Subexpression Elimination Algorithms - Difference Algorithms - Reconfigurable and Time-Multiplexed Multiple Constant Multiplications -Optimization Schemes and Optimal Algorithms - Optimal Sub expression Sharing-Representation Independent Formulations-Implementation of FIR Digital Filters and Filter Banks - Implementation of Sinusoidal and Other Linear Transforms .

MODULE V CORDIC PROCESSING 10

Basic CORDIC Techniques -The CORDIC Algorithm -Generalization of the CORDIC Algorithm- Multidimensional CORDIC- Advanced CORDIC Algorithms and Architectures -High-Radix CORDIC Algorithm-Angle Recoding Methods - Hybrid or Coarse-Fine Rotation CORDIC - Redundant Number-Based CORDIC Implementation - Pipelined CORDIC Architecture -Differential CORDIC Algorithm - Scaling, Quantization, and Accuracy Issues -Implementation of Mixed-Scaling Rotation - Low-Complexity Scaling - Quantization and Numerical Accuracy -Area-Delay-Accuracy Trade-off-Applications of CORDIC - Matrix Computation -Signal Processing and Image Processing Applications.

Total Hours : 45

TEXT BOOK

1. Pramod Kumar Meher, “Arithmetic Circuits for DSP Applications”,Wiley IEEE press, 2017.
2. Hongjiang Song,” Principles of VLSI Design - Symmetry, Structures and Methods”,Lulu Publishers, 2018.
3. Keshab K. Parhi. VLSI Digital Signal Processing Systems, Wiley-Inter Sciences, 1999

REFERENCES:

1. Keshap K. Parhi, VLSI Digital Signal Processing Systems, Design and Implementation, John Wiley, 2007.
2. U. Meyer – Baese, “Digital Signal Processing with Field Programmable Gate Arrays”, Springer, Second Edition, 2004.

OUTCOMES :

On completion of the course the student will be able to

- Describe various algorithms that can be designed and applied on application specific VLSI architecture
- Design fast convolution algorithms and high speed multipliers to improve the efficiency of DSP processors
- Develop advanced DSP filters and processors.
- DSP designs by employing the advantages of CORDIC VLSI concepts
- Understand the concepts of VLSI architectures for Time domain signal processing ,spatial and frequency domain signal processing
- Discuss the noise effect in VLSI spatial signal processing.

ECDY 063	DSP SYSTEM DESIGN	L	T	P	C
		2	0	0	2

OBJECTIVES:

The OBJECTIVES of the course is

- To describe the concept of Multirate Signal Processing
- Analyze the design issues in digital filter design, transform-domain processing and importance of Signal Processors.
- To study speech coding using Linear Prediction

PREREQUISITES :

The readers must have knowledge on basic Signal Processing Techniques.

MODULE I MULTIRATE SIGNAL PROCESSING 7

Decimation and Interpolation, Spectrum of Decimated and Interpolated Signals, Polyphase Decomposition of FIR Filters and Its Applications to Multirate DSP. Sampling Rate Converters, Sub-Band Encoder. Filter Banks,Uniform Filter Bank, Direct and DFT Approaches.

MODULE II MODEM 8

Introduction to ADSL Modem, Discrete Multitone Modulation and it's Realization Using DFT,QMF, Short Time Fourier Transform Computation of DWT Using Filter Banks, Implementation and Verification on FPGAs, DDFS- ROM LUT Approach, Spurious Signals Jitter, Computation of Special Functions Using CORDIC, Vector and Rotation Mode of CORDIC, CORDIC Architectures.

MODULE III SOFTWARE RADIO 8

Block Diagram of a Software Radio, Digital Down Converters and Demodulators, Universal Modulator and Demodulator Using CORDIC, Incoherent Demodulation - Digital Approach for I and Q Generation, Special Sampling Schemes, CIC Filters, Residue Number System and High Speed Filters Using RNS, Down Conversion Using Discrete Hilbert Transform, Under sampling Receivers, Coherent Demodulation Schemes.

MODULE IV SPEECH CODING 7

Speech Apparatus, Models of Vocal Tract, Speech Coding Using Linear Prediction, CELP Coder, An Overview of Waveform Coding, Vocoders, Vocoder Attributes,

Block Diagrams of Encoders and Decoders of G723.1, G726, G727, G728 and G729.

Total Hours : 30

TEXT BOOK

1. J. H. Reed, Software Radio, Pearson, 2002.
2. U. Meyer – Baese, Digital Signal Processing with FPGAs, Springer, 2004

REFERENCE BOOK

1. Tsui, Digital Techniques for Wideband receivers, Artech House, 2001.
2. S. K. Mitra, Digital Signal processing, McGrawHill, 1998

OUTCOMES :

On completion of the course the student will be able to

- Design of modem
- Design of high speed filters using redundant number system.
- Use of multirate processing
- Use various speech coders
- Applications of transforms in system modeling
- Implement and Verify DSP systems using FPGAs.

ECDY 064 ELECTRONIC DESIGN AUTOMATION TOOLS

L	T	P	C
2	0	0	2

OBJECTIVES:

The OBJECTIVES of the course is

- To know the basics of Electronic design tools.
- To study the concepts of simulation and synthesis of HDLs.
- To practice the concepts of SPICE and circuit simulation using Spice.
- To analyzes the concepts of S-edit.
- To design the Layout using S-edit

PREREQUISITES :

- VLSI Design

MODULE I BASICS OF EDA **7**

VLSI Design Automation tools-An overview of the features of practical CAD tools – Modelsim - Leonardo spectrum -Xilinx ISE - Quartus II - VLSI backend tools –IC Station, Cadence and Synopsis.

MODULE II SYNTHESIS OF HDLS **8**

Logic synthesis in Verilog – Logic synthesis in VHDL - Finite State Machines synthesis in Verilog – Finite State Machines synthesis in VHDL - Memory synthesis in Verilog – Memory synthesis in VHDL - Performance driven synthesis.

MODULE III SIMULATION OF SPICE **7**

Circuit description - DC circuit analysis- Transient analysis - AC circuit analysis - Advanced spice commands and analysis- Models for Semiconductor diodes - Models for Bipolar Junction Transistors - Models for Field Effect Transistors.

MODULE IV SCHEMATIC AND LAYOUT DESIGN **8**

Creating a project- Drawing, Selecting and Editing objects -Creating a schematic - Creating a symbol - Importing and Exporting Net lists and Schematics - Simulation and Waveform probing.

TOTAL HOURS: : 30

TEXT BOOKS

1. Louis Scheffer, Luciano Lavagno and Grant Martin, “Electronic Design Automation for Integrated Circuits Handbook, Volume 1, EDA for IC System

Design, Verification and Testing", Taylor & Francis, 2006.
2. Dennis Fitzpatrick, "Analog Design and Simulation using OrCAD Capture and PSpice", Newnes, 2nd edition, December 13, 2017.
3. Luca P.Carloni, Roberto Passerone, Allesandro Pinto and Alberto L.Sangiovanni,"Languages and Tools for Hybrid System design", Now publishers, 2006.
4. M.J.S.Smith, Application Specific Integrated Circuits, Pearson Education, 2008.
5. M.H.Rashid**,** Introduction to PSpice Using OrCAD for Circuits and Electronics, 3rd Edition, PHI 2003.

REFERENCES

1. Erik Brunvand, "Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Addison-Wesley, 2010.
2. J.Bhaskar, Verilog Synthesis Primer, Prentice Hall, 1998.
3. J.Bhaskar, A Verilog Primer, Prentice Hall, 2005

OUTCOMES:

On completion of the course the student will be able to

- Relate the basic definitions and overview of different tools.
- Express how to solve simulation, Synthesis of HDLs.
- Interpret and implement appropriate formulations and algorithms from SPICE.
- Create an appropriate method to design an S-edit.
- Plan the process of netlist and schematic creation.
- Design the layout of SPICE models

ECDY 065	PROGRAMMING SYSTEM VERILOG	L	T	P	C
		2	0	0	2

OBJECTIVES:

The OBJECTIVES of the course is

- Learn the basics of functional verification languages and to impart knowledge on the OOPS concepts
- Understand and use the System Verilog RTL design
- Learn the system verilog language constructs and the functional verification procedures
- Design state machines to control complex systems.
- Analyse and debug verilog modules.
- Write a verilog test bench to test verilog modules.

PREREQUISITES :

- A working knowledge of Verilog, A basic understanding of digital hardware design and verification

MODULE I INTRODUCTION TO FUNCTIONAL VERIFICATION LANGUAGES 7

Introduction to System Verilog, System Verilog data types. System Verilog procedures, Interfaces and modports, System Verilog routines.

MODULE II INTRODUCTION TO OBJECT ORIENTED PROGRAMMING 7

Classes and Objects, Inheritance, Composition, Inheritance v/s composition, Virtual methods. Parameterized classes, Virtual interface, Using OOP for verification, System Verilog Verification Constructs.

MODULE III SYSTEM VERILOG ASSERTIONS 8

Introduction to assertion, Overview of properties and assertion, Basics of properties and sequences, Advanced properties and sequences, Assertions in design and formal verification, some guidelines in assertion writing.

MODULE IV COVERAGE DRIVEN VERIFICATION AND FUNCTIONAL COVERAGE IN SV **8**

Coverage Driven Verification, Coverage Metrics, Code Coverage, Introduction to functional coverage, Functional coverage constructs, Assertion Coverage, Coverage measurement, Coverage Analysis SV and C interfacing: Direct Programming Interface (DPI)

Total Hours : 30

TEXT BOOKS:

1. Sutherland, Stuart, Davidmann, Simon, Flake “SystemVerilog for Design” : A Guide to Using SystemVerilog for Hardware Design and Modeling, Springer Science & Business Media, 2013
2. Chris Spear “SystemVerilog for Verification”: A Guide to Learning the Testbench Language Features, Springer Science & Business Media , 2012
3. Mintz, Mike, Ekendahl, Robert “Hardware Verification with System Verilog”: An Object-Oriented Framework, Springer Science & Business Media, 2007.

REFERENCES:

1. Bergeron, Janick “Writing Testbenches using SystemVerilog”, Springer Science & Business Media, 2012.
2. MeyyappanRamanathan “A Practical Guide for SystemVerilog Assertions”, Springer Science & Business Media, 2006

OUTCOMES :

On completion of the course the student will be able to

- Describe the OOPS concepts
- Describe system verilog syntax and language construct
- Write basic system Verilog constructs to verify digital systems
- Develop assertion constructs to verify digital systems
- Use EDA tools for formal verification
- Write system verilog constructs for convergence driven verification procedures

ECDY 066	SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION	L	T	P	C
		1	0	0	1

OBJECTIVES:

The OBJECTIVES of the course is to

- Learn the fundamentals of scripting languages to operate the EDA tools
- Study the basic syntax constructs of PERL scripts

MODULE I OVERVIEW OF SCRIPTING LANGUAGES 05

Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

MODULE II PERL 10

PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables. Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL.

L:15 - Total Hours:15

REFERENCES

1. Randal L, Schwartz Tom Phoenix, “Learning PERL”, Oreilly Publications, 3rd Edn., 2000
2. Larry Wall, Tom Christiansen, John Orwant, “Programming PERL”, Oreilly Publications, 3rd Edn., 2000
3. Tom Christiansen, Nathan Torkington, “PERL Cookbook”, Oreilly Publications, 3rd Edn,2000

OUTCOMES:

On completion of the course the students will be able to

- Describe the fundamentals of scripting languages
- Write basic scripts to operate EDA tools
- Apply scripting language like PERL to improve EDA tool flow
- Create scripts to synthesize Digital circuits using CAD tools

PROFESSIONAL ELECTIVES - EMBEDDED SYSTEMS

ECDY 025	WIRELESS SENSOR NETWORKS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To make the students list the Wireless Sensor Network Architecture and its Applications
- To explain the physical layer design,
- To describe the MAC protocols and time synchronization algorithms
- To discuss various routing protocols, localization algorithms used for sensor network.
- To explain basics of sensor network programming and Internet of Things

PREREQUISITES:

To know about the basic concepts of networking and protocol.

MODULE I NODE ARCHITECTURE 07

Introduction to sensor network – Application – Difference between Adhoc and Sensor Network - Node architecture - Hardware components overview - Energy consumption of Sensor nodes - Operating Systems and Execution Environment - some examples of Sensor nodes.

MODULE II NETWORK ARCHITECTURE 07

Sensor Network Scenarios – Optimization goals- Design Principles –Gateway Concepts–Wireless Channel fundamentals - Physical layer and transceiver design considerations in Wireless Sensor Network

MODULE III MAC PROTOCOLS & TIME SYNCHRONIZATION 10

Fundamentals of MAC Protocols – Low duty cycle protocols – Contention based Protocols – schedule based protocols – IEEE 802.15.4 MAC – Address and name management in wireless sensor network. Need for time synchronization

MODULE IV LOCALIZATION & ROUTING PROTOCOLS 12

Properties of localization and positioning procedures – Range based Localization – Range free Localization Routing Metrics – Data Centric Routing– Proactive Routing - On Demand Routing – Hierarchical Routing – QoS based Routing Protocols

MODULE V SENSOR NETWORK PROGRAMMING and IoT 09

Challenges in sensor network programming – Node Centric programming – Dynamic programming – Sensor Network Simulators - Internet of Things (IoT): overview, Applications, potential & challenges, and architecture.

Total Hours: 45

TEXT BOOKS:

1. Holger Karl and Andreas Willig, “Protocols and Architectures for Wireless Sensor Networks”, John Wiley and Sons, 2012.
2. WaltenegusDargie and Christian Poellabauer, “Fundamentals of Wireless Sensor Networks – Theory and Practice”, John Wiley and Sons, First edition, 2010.

REFERENCES:

1. G.Anastasi, Marco Conti, Mario Di Francesco and Andrea Passarella, “Energy Conservation in Wireless Sensor Networks: A Survey”, Adhoc Networks, Vol.7, No.3 May 2009, Elsevier Publications, pp.537-568.
2. “Adrian McEWen and Hakim Cassimalli, “Designing the Internet of Things” Wiley publications, November 2013.

OUTCOMES:

At the end of the course students will be able to

- Describe Wireless Sensor Network Architecture and its Applications
- Explain the physical layer design
- Compare the various MAC protocols and illustrate time synchronization algorithms
- Distinguish various routing protocols, localization algorithms used for sensor network.
- To describe the basics of sensor network programming and Internet of Things
- Analyze various Sensor Network Simulators

ECDY 034 SOFTWARE FOR EMBEDDED SYSTEMS

L	T	P	C
2	0	2	3

OBJECTIVES:

The OBJECTIVES of the course is

- To know the basic concepts of C Programming.
- To Introduce the GNU C Programming Tool Chain in Linux.
- To understand embedded C and Embedded OS
- To introduce the python language

PREREQUISITES :

- Embedded system

MODULE I C LANGUAGE PROGRAMMING 12

Basics of Program Writing-Declarations and Expressions-Arrays, Qualifiers-Control Statements- Functions-C Preprocessor, Bit Operations-Advanced Types- Advanced Pointers-Modular programming-Portability Problems-C's Dustier Corners

Laboratory Practice: Practice C language programs illustrating the language constructs in the module I using C compiler

MODULE II C PROGRAMMING TOOLCHAIN IN LINUX ENVIRONMENT 12

Introduction to GCC - Debugging with GDB - The Make utility - GNU Configure and Build System - GNU Binary utilities - Profiling - using gprof - Memory Leak Detection with valgrind - Introduction to GNU C Library .

Laboratory Practice: Practice C language programs using GCC compiler in Linux environment

MODULE III EMBEDDED C USING 8051 MICROCONTROLLER 12

Adding Structure to 'C' Code: Object oriented programming with C, Header files for Project and Port, Examples. Meeting Real-time constraints: Creating hardware delays - Need for timeout mechanism - Creating loop timeouts - Creating hardware timeouts.

Laboratory Practice: Practice Embedded C language programs illustrating the language construct in the module III using C Keil µvision IDE.

MODULE IV EMBEDDED OS 12

Creating embedded operating system: Basis of a simple embedded OS, Introduction to sEOS, Using Timer 0 and Timer 1, Portability issue, Alternative system architecture, and Important design considerations when using sEOS.

Laboratory Practice: Practice Embedded C language programs illustrating the language construct in the module IV using C Keil µvision IDE.

MODULE V PYTHON LANGUAGE 12

Basics of PYTHON Programming Syntax and Style – Python Objects– Dictionaries – Conditionals and Loops – Files – Input and Output – Errors and Exceptions – Functions – Modules – Classes and OOP.

Laboratory Practice: Practice basic Python language programs illustrating the language construct in the module V using Python interactive shell software.

Total Hours: 60

TEXT BOOKS:

1. Stephen Kochan, “Programming in C”, 3rd Edition, Sams Publishing, 2009.
2. Steve Oualline, ‘Practical C Programming 3rd Edition’, O’Reilly Media, Inc, 2006.

REFERENCES:

1. Michael J Pont, “Embedded C”, Pearson Education, 2007.
2. Mark Lutz, “Learning Python Powerful OOPs”,O’reilly,2011.

OUTCOMES :

On completion of the course, students will be able to:

- Write, compile and debug programs in C language.
- Compile the program in Linux platform.
- Develop program using embedded C
- Describe operating system in embedded system
- Program using python language
- Design projects using embedded C and python language

ECDY 024	INTERNET OF THINGS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To introduce emerging technological options and platforms
- To explain the architecture of IoT
- To explore application development for mobile Platforms
- To Provide the appropriate IoT solutions and recommendations according to the applications used.

PREREQUISITES:

- Computer networks
- Embedded system

MODULE I THE IoT NETWORKING CORE 9

History of IoT, Review of Technologies involved in IoT Development, Internet/Web and Networking Basics -OSI Model, Data transfer referred with OSI Model, IP Addressing, Point to Point Data transfer, Point to Multi Point Data transfer & Network Topologies, Sub-netting, Network Topologies referred with Web, Introduction to Web Servers, Introduction to Cloud Computing. Basics of Big Data, Data Science.

MODULE II IoT ARCHITECTURE AND APPLICATIONS 9

Architecture: M2M – Machine to Machine, Web of Things, IoTprotocol,Introduction to wireless and mobile networks,ZigBee, BLE mesh, WiFi, MQTT, LoRa-Machine Applications: Remote Monitoring & Sensing, Remote Controlling,Performance Analysis.

MODULE III IoT PLATFORM OVERVIEW 9

Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards. Network Fundamentals: Overview and working principle of Wired Networking equipment's – Router, Switches, Overview and working principle of Wireless Networking equipment's – Access Points, Hubs etc. Linux Network configuration Concepts: Networking configurations in Linux Accessing Hardware & Device Files interactions.

MODULE IV IoT APPLICATION DEVELOPMENT 9

Application Protocols-MQTT, REST/HTTP, CoAP, MySQL -Back-end Application -

Design Apache for handling HTTP Requests, PHP & MySQL for data processing, MongoDB Object type Database, HTML, CSS &jQuery for UI Designing, JSON lib for data processing, Security & Privacy during development, Application Development for mobile Platforms: Overview of Android / IOS 10 25 47 /97 App Development tools

MODULE V CASE STUDY & ADVANCED IoT APPLICATIONS 9

IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards.

Total Hours: 45

TEXT BOOKS:

1. Jean-Philippe Vasseur, Adam Dunkels, “Interconnecting Smart Objects with IP: The Next Internet”, Morgan Kuffmann-2010
2. Vijay Madisetti , ArshdeepBahga, : Internet of Things (A Hands-on-Approach)” -2014
3. Adrian McEwen (Author), Hakim Cassimally, “Designing the Internet of Things” ,Wiley -2013
4. Dr. OvidiuVermesan, Dr. Peter Friess, “Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems,” River Publishers -2013

REFERENCES:

1. Barrie Sosinsky, “Cloud Computing Bible”, Wiley-India, 2010
2. Asoke K Talukder and Roopa R Yavagal, “Mobile Computing,” Tata McGraw Hill, 2010.
3. Adelstein and S.K.S. Gupta, “Fundamentals of Mobile and Pervasive Computing,” McGraw Hill, 2009
4. Ronald L. Krutz, Russell Dean Vines “Cloud Security: A Comprehensive Guide to Secure Cloud Computing”, Wiley-India, 2010

OUTCOMES :

At the end of the course students will be able to

- Articulate the main concepts, key technologies, strengths, and limitations of cloud computing and the possible applications for state-of-the-art Internet of things
- Identify the architecture and infrastructure of IoT.
- Explain the core issues of IoT such as security, privacy, and interoperability
- Choose the appropriate technologies, algorithms, and approaches for the

related issues.

- Identify problems, and explain, analyze, and evaluate various IoT solutions
- Attempt to generate new ideas and innovations in IoT.

ECDY 072 CONTROLLER AREA NETWORK L T P C
3 0 0 3

OBJECTIVES:

The primary course Objectives are

- To introduce the fundamental concepts of embedded networking
- To provide overview of CAN controller.
- To acquire knowledge on CAN development tools.
- To know about CAN open configuration.
- To understand the implementation of CAN open.
- To explain the issues involved in CAN open implementation.

PREREQUISITES:

- Fundamentals of communication systems
- Basic knowledge about networks

MODULE I EMBEDDED NETWORK REQUIREMENTS 08

Embedded networking - Terminology used in Embedded Networking– code requirements – Communication requirements.

MODULE II CAN 09

Controller Area Network – Underlying Technology CAN Overview – Selecting a CAN Controller – CAN development tools.

MODULE III CAN OPEN 09

CAN open configuration – Evaluating system requirements choosing devices and tools – Configuring single devices – Overall network configuration – Network simulation – Network Commissioning – Advanced features and testing.

MODULE IV IMPLEMENTATION OF CAN OPEN 10

Implementing CAN open Communication layout and requirements – Comparison of implementation methods – Micro CAN open – CAN open source code – Conformance test – Entire design life cycle

MODULE V CAN OPEN IMPLEMENTATION ISSUES 9

Using CAN hardware in a CAN open context- Implementation of multiple device modules- Other software and hardware considerations- An example of CAN open based system integration.

L – 45; Total Hours: 45

TEXT BOOKS:

1. GlafP.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”. Embedded System Academy 2008.
2. Mohammed Farsi, Barbosa, “CANopen Implementation : Applications to Industrial Network (Industrial Control, Computers, and Communications Series,18),Research Studies Press,2000
3. Gregory J. Pottie, William J. Kaiser “Principles of Embedded Networked Systems Design”, Cambridge University Press, Second Edition, 2009.

REFERENCES :

1. D.Paret, “Multiplexed Networks for Embedded Systems”, John Wiley & Sons, 2014
2. Marco Di Natale, Haibo Zeng, Paolo Giusto, ArkadebGhosal ,“Understanding and Using the Controller Area Network Communication Protocol “,Springer publishers,2012
3. Konrad Etschberger,”**Controller Area Network**: Basics, Protocols, Chips and Application”, IXXAT Press, 2001.
4. Wilfried Voss,” A Comprehensible Guide to Controller Area Network”,Copperhill technologies corporation, 2008.

OUTCOMES:

On completion of the course, students will be able to

- Explain the requirements of embedded networking.
- Describe control area network and its development tools.
- Interpret the CAN message format.
- Determine system requirements for choosing devices and tools for CAN open.
- Use appropriate implementation methods in CAN open.
- Analyse the issues in implementation of CAN open.

ECDY 073 DISTRIBUTED EMBEDDED COMPUTING

L	T	P	C
3	0	0	3

OBJECTIVES:

The primary course Objectives are

- The various hardware and software architectures used for distributed embedded computing.
- Distributed computing system models and Distributed databases.
- The infrastructure required to support an Internet connection, uses of common Internet protocols, and basic principles of the DNS.
- The distributed computing technologies.

PREREQUISITES :

- Embedded system

MODULE I THE HARDWARE INFRASTRUCTURE 9

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.

MODULE II INTERNET CONCEPTS 9

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

MODULE III DISTRIBUTED COMPUTING 9

Definition- Model of distributed computation- Distributed shared memory- Authentication in distributed system.

MODULE IV EMBEDDED AGENT 9

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

MODULE V EMBEDDED COMPUTING ARCHITECTURE 9

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic

scheduling algorithm for real-time multiprocessor systems.

Total Hours 45

TEXT BOOKS:

1. Ajay D Kshemkalyani,MukeshSinghal, “Distributed Computing” – Principles, Algorithm and systems, Cambridge university press 2008
2. Dietel&Dietel, “JAVA-How to program”, Prentice Hall 2011.
3. SapeMullender, “Distributed Systems”, Addison-Wesley, 1993.
4. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub, 1997.
5. Bernd Kleinjohann “Architecture and Design of Distributed Embedded Systems”, C-lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, 2001.

REFERENCE BOOKS:

1. Pradeep K Sinha, “Distributed Operating Systems: Concepts and Design”, Prentice Hall of India, 2007.
2. Tanenbaum A.S., Van Steen M., —Distributed Systems: Principles and Paradigms‖, Pearson Education, 2007.

OUTCOMES :

On completion of the course the students will able to

- Describe the hardware infra structure of distributed embedded system
- Elucidate the architecture of embedded web server
- Able to understand the fundamentals of Network communication technologies and distributed computing.
- Designing and analyze high-performance Embedded system
- Analyze the performance of multiprocessor system on chip architecture
- Select suitable embedded architecture for distributed embedded system

ECDY 074	EMBEDDED NETWORKING	L	T	P	C
		3	0	0	3

OBJECTIVES:

. The primary course Objectives are

- To study the concepts of embedded networking
- To explore various bus architectures.
- To explore the fundamentals of embedded security.

PREREQUISITES :

- Embedded system

MODULE I THE AUTOMOTIVE CAN BUS 9

Introduction-Concepts of Bus Access and arbitration –error processing and management –definition of the CAN protocol ISO 11898-1-error properties-detection and processing –framing, signal propagation-Bit synchronization-high speed CAN –low speed CAN-CAN components and development tools for CAN.

MODULE II UNIVERSAL SERIAL BUS 9

USB bus –Introduction –Speed Identification on the bus – USB States –USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface –C Programs.

MODULE III INDUSTRIAL NETWORKING PROTOCOL 9

LIN – Local Interconnect Network - Basic concept of the LIN 2.0 protocol - Fail-safe SBC – Gateways - Managing the application layers - Safe-by-Wire - Safe-by-Wire Plus - Audio-video buses - I2C Bus - D2B (Domestic digital) bus - MOST (Media oriented systems transport) bus - IEEE 1394 bus or 'FireWire'- profi bus.

MODULE IV ETHERNET BASICS 9

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

MODULE V BLUETOOTH AND ZIGBEE 9

Bluetooth: Specifications- Bluetooth Radio- Type of Antenna, Antenna Parameters-

Bluetooth Networking- Wireless networking, wireless network types, devices roles and states – IEEE 802.15.4 –Zigbee specifications-.IRF Communication-Adhoc network, scatter net- GSM- Overview of IrDA, HomeRF, Wireless LANs- IEEE 802.11x – NFC.

Total Hours: 45

TEXT BOOKS:

1. Dominique Paret, "Multiplexed Networks for Embedded Systems", Wiley 2007.
2. Jan Axelson, "USB Complete", Lakeview Research, 2005
3. Jan Axelson, "Embedded Ethernet Complete", Lakeview Research, 2005.
4. GlafP.Feiffer, Andrew Ayre and Christian Keyold, "Embedded networking with CAN and CAN open". Embedded System Academy 2005.

REFERENCES:

1. Gregory J. Pottie, William J. Kaiser "Principles of Embedded Networked Systems Design", Cambridge University Press, Second Edition, 2005.
2. C.S.R. Prabhu and A.P. Reddi ,"Bluetooth Technology and its Applications with JAVA and J2EE, PHI, 2006
3. Rappaport Theodore S, "Wireless Communications: Principles And Practice", Pearson Education,2010
4. ShahinFarahani,b, "ZigBee Wireless Networks and Transceivers", Newnes Publications, 2008

OUTCOMES :

On completion of the course the students will able to

- Describe the components and significance of Embedded networking system
- Elucidate the principles of USB communications
- Create Embedded Ethernet controller
- Explain industrial networking protocols like I2C,D2B
- Use appropriate interfaces, protocols and buses in embedded systems
- Describe the architecture of Bluetooth and RF communication modules

ECDY 075	EMBEDDED LINUX	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn fundamentals of embedded linux.
- To familiarize the use of GNU tool chain.
- To develop embedded applications in linux platform.
- To understand open source BOSS Linux platform.

PREREQUISITES :

- Embedded system
- Operating system

MODULE I LINUX FUNDAMENTALS 9

Introduction - host-target development setup - hardware support -development languages and tools – RT Linux.

MODULE II KERNEL INITIALIZATION& DEVICE HANDLING 9

Linux kernel and kernel initialization - system initialization – hardware support - boot loaders- driver basics - module utilities - file systems - MTD subsystems – busy box

MODULE III DEVELOPMENT TOOLS 9

Embedded development environment - GNU debugger - tracing & profiling tools - binary utilities - kernel debugging - debugging embedded Linux applications - porting Linux - Linux and real time - SDRAM interface

MODULE IV DEVICE APPLICATIONS 9

Asynchronous serial communication interface - parallel port interfacing -USB interfacing - memory I/O interfacing - using interrupts for timing.

MODULE V OPEN SOURCE -BOSS LINUX OS 9

BOSS Linux Desktop- Synaptic Package Manager- Basic Commands- General Purpose Utilities- File System- Redirection Pipes-Process- Linux Environment- Basics of System Administration-Simple filters- grep command- sed command- Basics of awk.

Total Hours: 45

TEXT BOOKS

1. KarimYaghmour, Jon Masters, Gillad Ben Yossef, Philippe Gerum, “Building Embedded linux systems”, O'Reilly, 2008.
2. Christopher Hallinan, “Embedded Linux Primer: A practical real world approach”, Prentice Hall, 2007.
3. P. Raghavan, Amol Lad, SriramNeelakandan, “Embedded Linux System Design and Development”,Auerbach Publications, Taylor and Francis Group, 2006.

REFERENCES

1. Alan Cox, Sreekrishnan , Venkateswaran ,”Essential Linux Device Drivers” , 1st Edition, Prentice Hall, 2008
2. Craig Hollabaugh, “Embedded Linux - Hardware, Software and Interfacing”, Pearson Education, 2002.
3. Robert Love ,”Linux Kernel Development”, Pearson Education India, 2010

OUTCOMES :

At the end of the course students will be able to

- Explain RT linux fundamentals
- Identify difference between RT linux and embedded linux versions
- Analyze kernel and system initialization and porting Linux
- Debug and develop embedded linux applications
- Explain device handling in linux OS.
- Describe the BOSS linux commands

ECDY 076 HARDWARE-SOFTWARE CO-DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

The OBJECTIVES of the course is to

- Introduce the basics of hardware software Co-design.
- Describe the modeling concepts in Co-design.
- Explain the applications of models.
- Apply object oriented techniques in Co-Design process.

PREREQUISITES:

- FPGA architecture, Embedded System

MODULE I INTRODUCTION 09

Motivation hardware & software co-design, system design consideration, research scope & overviews Hardware Software back ground: Embedded systems, models of design representation, the virtual machine hierarchy, the performance3 modeling, Hardware Software development

MODULE II HARDWARE / SOFTWARE CO-SYNTHESIS 09

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.

MODULE III METHODOLOGY FOR CO-DESIGN 09

Amount of unification, general consideration & basic philosophies, a framework for co-design Unified Representation for Hardware & Software: Modeling concepts. Requirement & applications of the models, models of Hardware Software system, generality of the model Performance Evaluation: Application of the abstract Hardware & Software model, examples of performance evaluation.

MODULE IV OBJECT ORIENTED TECHNIQUES IN HARDWARE DESIGN 09

Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, and Processor example.

MODULE V SYSTEM ON CHIP 09

The System-on-Chip Concept, Four Design Principles in SoC Architecture,

SoCModeling in GEZEL. Applications: Trivium Crypto-Coprocessor, CORDIC Co-Processor.

L: 45 - Total Hours:45

TEXT BOOKS :

1. Jorgen Staunstrup, Wayne Wolf ,"Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub,1997.
2. Giovanni De Micheli , Rolf Ernst Morgon," Reading in Hardware/Software Co-Design "Kaufmann Publishers,2001.
3. Peter Marwedel, G. Goosens, "Code Generation for Embedded Processors", Kluwer Academic Publishers, 2002.
4. Ralf Niemann, Hardware/Software Co-Design for Data flow Dominated Embedded Systems, Springer, 1998

REFERENCES:

1. Sanjaya Kumar, James H. Ayler "The Co-design of Embedded Systems: A UnifiedHardware Software Representation", Kluwer Academic Publisher, 2002
2. H. Kopetz, "Real-Time Systems", Kluwer, 1997.
3. R. Gupta, "Co-synthesis of Hardware and Software for Embedded Systems", Kluwer 1995.
4. S. Allworth, "Introduction to Real-time Software Design", Springer-Verlag, 1984.
5. C. M. Krishna, K. Shin, "Real-time Systems", Mc-Graw Hill, 1997.

OUTCOMES:

At the end of the course students will be able to

- Describe the design methodologies used in the hardware software co-design
- Identify the core issues in co-design
- Describe the functions of co-design
- Assess the benefits of unified representation
- Evaluate the performance of the model
- Apply object oriented techniques in Hardware Design

ECDY 077 REAL TIME SYSTEMS L T P C

3 0 0 3

OBJECTIVES:

- To introduce the fundamental concepts of real time systems
- To know about scheduling algorithms applied for real time systems
- To acquire knowledge on programming languages and tools for real time systems.
- To provide overview of real time data bases.
- To understand the implementation of real time communication protocols.
- To explain the Fault Tolerance and evaluation techniques in real time systems.

PREREQUISITES:

- Fundamentals of operating systems
- Basic knowledge embedded systems.

MODULE I INTRODUCTION TO REAL TIME SYSTEM 09

Introduction –characterizing real time system -Performance Measures for Real Time Systems – Estimating Program Run Times – Task Assignment and Scheduling.

MODULE II PROGRAMMING LANGUAGES AND TOOLS 09

Desired language characteristics – Data typing – Control structures – Facilitating Hierarchical Decomposition- Packages- Run time Error handling – Overloading and Generics – Multitasking – Timing Specifications – Programming Environments – Run time support.

MODULE III REAL TIME DATABASES 09

Basic Definition, Real time Vs General Purpose Databases- Main Memory Databases- Transaction priorities-Transaction Aborts-Concurrency control issues-Disk Scheduling Algorithms-Two – phase Approach to improve Predictability – Maintaining Serialization Consistency – Databases for Hard Real Time Systems

MODULE IV REAL TIME COMMUNICATION 09

Communications media, Network Topologies, Protocols- contention based, Token based, Stop-and-Go multihop, Polled Bus, Hierarchical Round Robin Protocol, Deadline-Based Protocols, Fault Tolerant Routing.

MODULE V FAULT TOLERANT AND EVALUATION TECHNIQUES 09

Fault Tolerance Techniques – Fault Types – Fault Detection-Fault and Error containment- Redundancy- Reliability Evaluation Techniques – Obtaining parameter values- Reliability models for Hardware Redundancy – Software error models.

L – 45; Total Hours 45

TEXT BOOKS:

1. C.M. Krishna, Kang G. Shin, “Real – Time Systems”, McGraw – Hill International Editions, 2010
2. Rajib Mall, ”Real-time systems: theory and practice”, Pearson Education, 2007
3. Peter D.Lawrence, “Real Time Micro Computer System Design – An Introduction”, McGraw Hill, 1988.

REFERENCES:

1. Xiaocong Fan, “Real-Time Embedded Systems: Design Principles and Engineering Practices”, Elsevier, 2015
2. Albert M. K. Cheng, “Real-Time Systems: Scheduling, Analysis, and Verification“ Wiley publishers,2003
3. Stuart Bennett, “Real Time Computer Control – An Introduction”, Prentice Hall of India, 1998.
4. S.T. Allworth and R.N.Zobel, “Introduction to real time software design”,Macmillan,1987

OUTCOMES:

On completion of the course, students will be able to

- Explain the characteristics of real time system
- Apply scheduling algorithms based on the application
- Discuss about the programming language characteristics and tools of real time systems.
- Describe the real time data bases
- Illustrate the real time communication protocols.
- Analyze the Fault Tolerance and evaluation techniques in real time systems.

ECDY 078 RISC PROCESSOR ARCHITECTURE AND PROGRAMMING

L	T	P	C
3	0	0	3

OBJECTIVES:

The OBJECTIVES of the course is to

- Compare CISC and RISC processor architectures
- Understand AVR microcontroller architecture, memory organization and programming
- Introduce MSP430 processor architecture and programming
- Familiarize ARM processor architecture and programming
- To impart knowledge on the WSN application development using RISC processor

PREREQUISITES :

- Basic knowledge in Microprocessors and Microcontrollers.

MODULE I AVR MICROCONTROLLER ARCHITECTURE 9

Architecture – memory organization – addressing modes – instruction set – programming techniques –Assembly language & C programming-Development Tools – Cross Compilers – Hardware Design Issues.

MODULE II MSP430 ARCHITECTURE AND PROGRAMMING 9

Architecture – CPU features – Memory structure - Interrupts – Input and Output– On-chip peripherals – Addressing modes – Instruction sets – Hardware considerations – Flash memory – Programming in Low power design.

MODULE III ARM ARCHITECTURE AND PROGRAMMING 9

ARM processor fundamentals – Registers – Pipeline – Exceptions – Interrupts– core extension- Instruction set – Thumb instruction set - 'C' programming –writing and optimizing ARM assembly code – Instruction scheduling – Registerallocation – conditional execution – Looping constraints.

MODULE IV ARM APPLICATION DEVELOPMENT 9

Exception Handling – Interrupts – Interrupt handling schemes- Firmware and boot loader – Example: Standalone - Embedded Operating Systems –Fundamental Components - Example Simple little Operating System.

MODULE V DESIGN WITH ARM MICROCONTROLLERS 9

Case Studies: Application of ARM processor - embedded system for pedestrian dead reckoning, ARM-based SoC for routing in Wireless Sensors Networks, Wireless sensor networks: A survey on monitoring water quality.

Total Hours 45

TEXT BOOKS:

1. Muhammad Ali Mazidi, SarmadNaimi, SepehrNaimi, “AVR Microcontroller and Embedded Systems : Using Assembly and C” ,1st Edition, 2014.
2. Dananjay V. Gadre “Programming and Customizing the AVR microcontroller”,McGrawHill 2001
3. Chris Nagy, “Embedded systems design using the TI MSP430 series”, Elsevier 2003.

REFERENCES:

1. Steven Barrett and Daniel Pack, “Microcontroller Programming and Interfacing: Texas Instruments MSP430”, 1st edition, 2011.
2. Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield “ARM System Developer’s Guide Designing and Optimizing System Software”, Elsevier, 2007.
3. Steve Furber, “ARM system on chip architecture”, Addison Wesley, 2000.

OUTCOMES :

On completion of the course, students will be able to:

- Analyze the features of CISC and RISC processor architectures
- Develop simple application program using AVR microcontroller
- Integrate low power modes with embedded system application
- Implement scheduling mechanism in ARM processor.
- Use simple little operating system for suitable applications.
- Employ RISC processor in the applications of WSN.

ECDY 079	INDUSTRIAL AUTOMATION USING PLC, DCS AND SCADA	L	T	P	C
		3	0	2	4

OBJECTIVES:

- To introduce emerging technological options and platforms for industrial automation
- To explain the architecture of PLC, DCS AND SCADA
- To explore application development for industrial automation
- To provide the appropriate automation solutions and recommendations according to the applications.

PREREQUISITES:

- Basic knowledge in Micro-controllers, Control Systems

MODULE I PROGRAMMABLE LOGIC CONTROLLER: HARDWARE AND BASIC OPERATIONS 09

Hard relay logic, Evolution of Programmable logic controller (PLC), Hardware Components of PLC: Input/Output modules, power supplies, isolators, CPU, memory and programming devices. Generic Control system Architecture and IO Assignments, General PLC programming procedures, Developing fundamental ladder logic programs (as per IEC61131) for Boolean operations, PLC basic functions : Register basics, timer functions, counter functions.

MODULE II PROGRAMMABLE LOGIC CONTROLLERS: ADVANCED OPERATIONS, INSTALLATIONS AND TROUBLESHOOTING 09

Developing program control instructions, data manipulation instructions, math instructions, sequencer and shift register instructions, Functional block diagram, Analog control using PLC (PID control configuration, PLC installations and troubleshooting

MODULE III DISTRIBUTED CONTROL SYSTEM 07

Introduction to Distributed control system, DCS architectures, Comparison, Local Control Unit, Process interfacing issues, Operator interfaces - Low level and high level operator interfaces - Operator displays - Engineering interfaces - Low level and high level engineering interfaces, Latest trends and developments.

MODULE IV DATA ACQUISITION SYSTEMS 07

Computers in Process control – Data Loggers – Data acquisition systems (DAS) – Alarms – Direct Digital Control (DDC) - Characteristics of digital data – Controller software – Computer Process interface for Data Acquisition and control –Supervisory Digital Control (SCADA) -introduction and brief history of SCADA – SCADA Hardware and software.

MODULE V NETWORKING 07

Signal Conditioners and Its interfaces

LABORATORY: 21

1. Development of Ladder program for simple on-off applications.
2. Development of Ladder program for Timing and counting applications.
3. Automatic control of level using PLC.
4. Automatic control of temperature using PLC.
5. Control of pressure loop using PLC.
6. Configuring Screens and Graphics (DCS).
7. Programming of HMI interfacing with PLC.
8. Tag Assignments to Field Devices in DCS.
9. DCS based PID control for level loop.
10. Communicate PLC with SCADA.

L:39, P:21 - Total Hours:60

TEXT BOOKS:

1. W. Bolton, "PLC", Elsevier Newnes 4 John W. Webb Ronald &Areis "PLC"
2. Clarke, G., Reynders, D. and Wright, E., "Practical Modern SCADA Protocols: DNP3, 60870.5 and Related Systems", Newnes, 1st Edition, 2004.

REFERENCES:

1. Petrezeulla," Programmable Controllers", Mc-Graw Hill, 1989.
2. Michael P.Lucas, "Distributed Control System", Van Nastrand Reinhold Company, New York,1986.

OUTCOMES:

At the end of the course the student will be able to

- Articulate the main concepts, key technologies, strengths, and limitations of industrial automation
- Identify the architecture and infrastructure of PLC.

- Explain the core issues of PLC, DCS AND SCADA
- Choose the appropriate technologies, algorithms, and approaches for the related issues.
- Identify problems, and explain, analyze, and evaluate various automation solutions.
- Attempt to generate new ideas and innovations in industrial automation.

ECDY 080	SENSORS LAB	L	T	P	C
		0	0	2	1

OBJECTIVES:

The OBJECTIVES of the course is to

- Introduce different types of sensors
- Learn how to condition the sensor signal
- Study the operations of the sensors

PREREQUISITES:

Basic Electronics ,Instrumentation

LIST OF EXPERIMENTS

1. To study characteristics of photosensor and its applications.
2. To study the operation and measurement of thermocouple sensors and to estimate their response times.
3. To study the operation of piezoelectric sensors and its applications.
4. To study the operation of sound sensors and its applications.
5. To study the operation of force sensitivity sensors and analyze the parameters.

Labs incorporate implementation concerns involving interference, isolation, linearity, amplification, and grounding.

OUTCOMES:

On completion of the course, students will be able to:

- Design and build a temperature control system using analog hardware.
- Measure several sensors and choose one appropriate for the system they are designing and building.
- Measure the sensor output and do the appropriate conversions.
- Identify the sensor for specific application
- Analyze the behavior of the sensors
- Develop the embedded system based application

ECDY 081	MULTICORE ARCHITECTURE	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study multicore architecture and its importance.
- Get an insight of parallel programming for multicore architecture designs.
- To know shared memory functionality in multi core architecture.

PREREQUISITES :

- VLSI Design, Basics of Electronic circuit

MODULE I INTRODUCTION TO MULTI CORE ARCHITECTURES 9

Why Parallel Architecture - Convergence of Parallel Architectures- Fundamental Design Issues.

MODULE II PARALLEL PROGRAMS 9

Parallel Application Case Studies - The Parallelization Process - Parallelization of an Example Program.

MODULE III WORKLOAD-DRIVEN EVALUATION 9

Scaling Workloads and Machines - Evaluating a Real Machine - Evaluating an Architectural Idea or Tradeoff - Illustrating Workload Characterization

MODULE IV SHARED MEMORY MULTIPROCESSORS 9

Cache Coherence - Memory Consistency - Design Space for Snooping Protocols - Assessing Protocol Design Tradeoffs – Synchronization - Implications for Software.

MODULE V SCALABLE MULTIPROCESSORS 9

Scalability - Realizing Programming Models - Physical DMA - User-level Access - Dedicated Message Processing - Shared Physical Address Space - Clusters and Networks of Workstations - Comparison of Communication Performance - Synchronization

Total Hours: 45

TEXT BOOK:

1. David E. Culler, Jaswinder Pal Singh, “Parallel computing architecture: A hardware/software approach”, Morgan Kaufmann Elsevier Publishers, 1st edition, 1999.
2. Shameem Akhtar and Jason Roberts, “Multi-core Programming”, 2nd Edition, Intel Press, 2006.

REFERENCE BOOK:

1. Peter S. Pacheco, "An Introduction to Parallel Programming", Elsevier,1st edition, 2011

OUTCOMES :

On completion of the course the student will be able to

- Study the need of multicore architecture
- Explore parallel programming capability to design multicore architecture
- Study the work load balancing of multicore architecture
- Shared memory architecture’s flexibility
- Scalable multi core architectures for user’s flexibility
- Discuss the existing multicore architecture

ECDY 082 EMBEDDED SYSTEM FOR ROBOTICS

L	T	P	C
3	0	0	3

OBJECTIVES:

- To give an overview of embedded systems
- To provide an introductory understanding of robotics
- To learn about the robotic operating systems
- To familiarize with various sensors and actuators
- To equip the students with the fundamental knowledge on developing robots using the ROS
- To enable students to develop embedded robotics.

PREREQUISITES:

Embedded Systems, Operating Systems

MODULE I BASICS OF EMBEDDED SYSTEMS 9

Robots and Embedded Systems-Sensors - Sensor Categories, Binary Sensor, Analog versus Digital Sensors, Shaft Encoder; A/D Converter, Position Sensitive Device; Compass, Gyroscope, Accelerometer, Inclinometer, Digital Camera. Actuators - DC Motors, H-Bridge, Pulse Width Modulation, Stepper Motors, Servos. Control - On-Off Control, PID Control, Velocity Control and Position Control, Embedded Controllers, Interfaces

MODULE II BASICS OF ROBOTICS 9

Introduction-Robot Kinematics - Degree of Freedom - Forward Kinematics - Algebraic Solution - Inverse Kinematics - Robots and Sensors - Robots and Motors - Frames and Materials - Types of Robots

MODULE III INTRODUCTION TO ROBOT OPERATING SYSTEM 9

Installation of ROS - The ROS Graph - roscore - rosrun - Names, Namespaces and Remapping - roslaunch - Topics - Publishing a Topic, Subscribing a Topic - Latched Topics - Mixing Publishers and Subscribers - Services – Actions

MODULE IV ROBOTS AND SIMULATORS 6

Robots and Simulators - Subsystems - Actuation: Mobile Platform & Manipulator Arm - Sensor Head - Visual Camera - Depth Camera - Laser Scanner - Shaft Encoders - Computation - Actual Robots - PR2 - Robonaut 2 - Turtlebot - Baxter - Simulators - Stage – Gazebo.

MODULE V DEVELOPING ROBOTS WITH ROS 9

Wanderbot - Telepot Bot - Building Maps of the World

Total Hours: 45

TEXT BOOKS:

1. Thomas Bräunl, “Embedded Robotics: Mobile Robot Design and Applications with Embedded Systems”, Third Edition, Springer-Verlag Berlin Heidelberg, 2008.
2. Nilanjan Dey, Amartya Mukherjee, “Embedded Systems and Robotics with Open Source Tools” CRC Press, 2016
3. Morgan Quigley, Brian Gerkey, and William D. Smart, “Programming Robots with ROS”, O’Reilly, 2015.

REFERENCES:

1. R.K.Mittal and I.J.Nagrath, “Robotics and Control”, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2003.
2. John J. Craig, “Introduction to Robotics: Mechanics and Control”, Third Edition, Pearson/Prentice Hall, 2005.
3 .AnisKoubaa, "Robot Operating System (ROS) The Complete Reference”, First Volume, Springer, 2016.
4. K.S. Fu, R.C. Gonzalez and C.S.G. Lee, “Robotics: Control, Sensing, Vision, and Intelligence”, McGraw-Hill, New York, 1987.

OUTCOMES:

On completion of the course, students will be able to

- Understand the basics of embedded programming and robotics
- Identify different types, components, and configurations of various robot designs
- Be able to calculate the forward kinematics and inverse kinematics
- Use the latest in software programs to model, program, and control robots
- Write algorithms to program and control simple mobile robots in useful engineering applications
- Interpret data obtained from real life problems using appropriate techniques to select suitable sensors and actuators for robots

ECDY 083 NETWORK ON CHIP

L	T	P	C
3	0	0	3

OBJECTIVES:

- To introduce the concept of NoC.
- To study the architectures and protocols of Router.
- To identify the types of fault and study the performance analysis of router.

PREREQUISITES :

- Computer architecture

MODULE I INTRODUCTION TO INTERCONNECTION NETWORKS 9

Introduction-Uses of Interconnection Networks-Network Basics-Interconnection Network-Topology Basics

MODULE II TYPES OF NETWORKS 9

Butterfly-torus-non blocking-slicing and dicing-case studies

MODULE III BASICS OF ROUTING MECHANISM 9

Routing Basics-Oblivious Routing-Adaptive Routing-Routing Mechanics-flow control-deadlock and livelock

MODULE IV ROUTER ARCHITECTURE 9

Basic Router Architecture-Datapath Components-Arbitration-Allocation-Network interface-Error control

MODULE V ROUTER PERFORMANCE ANALYSIS 9

QoS-Measures of Interconnection Network Performance-Analysis-Validation-simulation-case study

Total Hours: 45

TEXT BOOKS:

1. William J. Dally, Brian P. Towles ,"Principles and Practices of Interconnection Networks , Elsevier ,2004
2. Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, "Low power NoC for high performance SoC desing",CRCpress,2008.

REFERENCES:

1. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-on – Chip " Architectures A Holistic Design Exploration", Springer,2010
2. Fayezgebali, Haythamelmiligi, HqhahedWatheq E1-Kharashi "Networks-on-Chips theory and practice CRC press,2017.

OUTCOMES :

- Understand the concepts of interconnection in network on chip
- Identify the need of NoC in multicore architecture
- Describe the different router architecture
- Design the components of NoC
- Develop the efficient router algorithm
- Analyze the performance of router

ECDY 084 INTEROPERABILITY CHALLENGES IN INTERNET OF THINGS

L	T	P	C
3	0	0	3

OBJECTIVES:

- To introduce the concept and characteristics of IoT interoperability.
- To discuss various middleware protocols used in IOT for connecting with different end devices and the challenges related to device interoperability
- To discuss wired and various short-range wireless networks related to devices interoperability
- To discuss on the types of interoperability and its key aspects
- To discuss on Interoperability Testing and the related performance challenges in a larger ecosystem

PREREQUISITES :

- Computer Networks

MODULE I INTRODUCTION 9

Introduction to IoT and its Interoperability challenges - Characteristics for IoT interoperability - barrier for adoption of lifestyle - Network connectivity – Middleware Protocols considered for interoperability - Types of Interoperability Connectivity; Technical; Syntactic; Semantic; Interoperability at Present state - Key Challenges - IoT Interoperability in a nutshell.

MODULE II INTEROPERABILITY STANDARDS 9

Interoperability Standards – onem2m; OPC; dot dot; OCF/ IoTivity; design Aspects for handling interoperability on devices, gateways and cloud; Open source software enabling interoperability; End-2-End system design for IoT interoperability; Interoperability between various service domains in a smart city

MODULE III PROTOCOLS 9

Middleware/Application protocols for handling IOT interoperability–Wi-Fi; Bluetooth; SIP; ZigBee; ZWave; CoAP; 6LowPAN; MQTT; DLNA; UPnP; HAP; RTSP; CAN; HART; MODBUS; RESTful; HTTP(s); MTP, RTP/ RTCP, HLS, MPEG-DASH, HTTP-PD; Home device products, Google Nest; Amazon-Echo; Philips-Bulbs; IKEA–Bulbs;August-Locks; Lockitron-Locks; Lifxulbs; Honeywell; Samsung; Grand stream; LG; Sony and the Interworking challenges.

MODULE IV CLOUD COMPUTING 9

Cloud Computing Architecture - Need for Cloud Computing Interoperability - Layers of interoperability in Cloud Computing - Levels of cloud computing interoperability - Major Concerns in Cloud Computing Interoperability - Approaches to solve interoperability issues

MODULE V TESTING AND APPLICATIONS 9

Interoperability Testing - Benefits; Challenges – Applications and Use cases- Smart Home; Industrial IOT; Smart City; Connected Vehicles; Logistics; A vision of future for IoT interoperability - Bridging the Interoperability Gap of the IoT; to standardize the Interoperability as an M3 protocol (Multi-vendor, Multi-device and Multi-domain).

Total Hours: 45

TEXT BOOKS:

1. Jean-Philippe Vasseur, Adam Dunkels, “Interconnecting Smart Objects with IP: The Next Internet”**,** Morgan Kuffmann, 2010
2. Dimitrios Serpanos, Marilyn Wolf, “Internet-of-Things (IoT) Systems Architectures, Algorithms, Methodologies”, Springer International Publisher, 2018.
3. Ovidiu Vermesan, Peter Friess, ““Internet-of-Things – From Research and Innovation to Market Deployment”, River Publishers, Series in Communications, 2014.

REFERENCES:

1. Arne Broring, et al, “Advancing IoT Platforms Interoperability”, IoT European Platform Initiative, River Publishers, 2018.
2. Ovidiu Vermesan and Peter Friess, “Digitizing the industry Internet of Things Connecting the Physical, Digital and Virtual Worlds”, River Publishers, Series in Communications, 2016.

OUTCOMES :

On completion of the course, students will be able to:

- Apply the concept of Interoperability in IOT networks.
- Identify the design challenges and the issues related to interoperability in various verticals.

- Analyze the middleware protocol issues
- Evaluate the necessity and need of having interoperability framework.
- Design and select the interoperability framework.
- Describe the limitations of interoperability and to apply in specific application

ECDY 085 EMBEDDED AUTOMOTIVE SYSTEM

L	T	P	C
3	0	0	3

OBJECTIVES:

- To describe the automotive electronics
- To utilize the automotive systems in automobiles.
- To explore the new trends in automotive industry
- To understand the applications of embedded systems in automotive industry.

PREREQUISITES :

- Embedded Systems

MODULE I ELECTRONICS IN THE AUTOMOBILE 9

Introduction- Body and convenience electronics: vehicle power supply controllers and lighting MODULEs, door control MODULEs, Safety electronics: active safety systems: ABS, ASR, ESP, passive safety systems: Restraint systems and their associated sensors in an automobile. Power train Electronics: Gasoline engine management, Infotainment electronics: Dashboard/instrument cluster, car audio, telematics systems, navigation systems, multimedia systems, cross application technologies.

MODULE II AUTOMOTIVE COMMUNICATION PROTOCOLS 9

CAN bus - Concepts of bus access and arbitration - Error processing and management - Definitions of the CAN protocol: 'ISO 11898-1' - Errors: their intrinsic properties, detection and processing – Physical layer, Application layers and development tools for CAN – LIN - Basic concept of the LIN 2.0 protocol.

FlexRay - Event-triggered and time-triggered aspects - TTCAN – Time-triggered communication on CAN- Towards high-speed, X-by-Wire and redundant systems – FlexRay

MODULE III AUTOMOTIVE EMBEDDED SYSTEMS 9

Automotive Embedded systems. Microcontroller in Automobile applications - Different Types of Microcontrollers in Automotive systems – Challenges in ECU design - Growth in the Automobile – Application in Vehicle Control - Power train - Driver Information – Steering – Telematics

MODULE IV DRIVE BY WIRE 9

Challenges and opportunities of X-by-wire: system & design requirements, steer-by-wire, brake- by-wire, suspension-by-wire, gas-by-wire, power-by-wire, shift by wire. Future of Automotive Electronics.

MODULE V AUTOSAR 9

AUTOSAR Architecture- Basic concepts- Software components - Layered Architecture - Microcontroller Abstraction Layer – ECU Abstraction Layer - Complex Device Driver - Service Layer – RTE - Application Layer - Basic Software MODULEs – Diagnostics - Methodology - Tools in SW development using Autosar- EB tresos Studio.

Total Hours : 45

TEXT BOOKS:

1. D.Paret, “Multiplexed Networks for Embedded Systems”, John Wiley & Sons, 2014
2. Marco Di Natale, Haibo Zeng, Paolo Giusto, Arkadeb Ghosal, “Understanding and Using the Controller Area Network Communication Protocol “, Springer publishers,2012

REFERENCESs:

1. Konrad Etschberger,”**Controller Area Network**: Basics, Protocols, Chips and Application”, IXXAT Press, 2001.
2. GlafP.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”, Embedded System Academy 2008.

OUTCOMES :

On completion of the course the student will be able to

- Design and develop automotive embedded systems.
- Analyze various embedded products used in automotive industry.
- Implement CAN and LIN protocol
- Evaluate the opportunities involving technology, a product or a service required for developing a start-up idea used for automotive applications
- Interface devices and build a complete system.
- Analyze the features of AUTOSAR Architecture.

GENERAL ELECTIVES

GEDY 101 PROJECT MANAGEMENT L T P C
3 0 0 3

OBJECTIVES:

The objectives of the course would be to make the students

- Learn to evaluate and choose an optimal project and build a project profile.
- Attain knowledge on risk identification and risk analysis
- Gain insight into a project plan and components
- Familiar with various gamut of technical analysis for effective project implementation
- Learn to apply project management techniques to manage resources.

MODULE I INTRODUCTION & PROJECT INITIATION 09

Introduction to project and project management - projects in contemporary organization – The project life cycle - project initiation - project evaluation methods & techniques - project selection criteria - project profile.

MODULE II RISK ANALYSIS 09

Sources of risk: project specific - competitive - industry specific - market and international risk – perspectives of risk – risk analysis: sensitivity analysis - scenario analysis - breakeven analysis - simulation analysis - decision tree analysis – managing/mitigating risk – project selection under risk.

MODULE III PROJECT PLANNING & IMPLEMENTATION 09

Project planning – importance – functions - areas of planning - project objectives and policies - steps in planning process - WBS – capital requirements - budgeting and cost estimation - feasibility analysis - creation of project plan – project implementation: pre-requisites - forms of project organization

MODULE IV TECHNICAL ANALYSIS 09

Technical analysis for manufacturing/construction/infrastructure projects – process/technology - materials and inputs - product mix - plant capacity – plant location and site selection – plant layout - machinery and equipment – structures and civil works – schedule of project implementation – technical analysis for software projects.

MODULE V PROJECT MANAGEMENT TECHNIQUES 09

Project scheduling - network construction – estimation of project completion time – identification of critical path - PERT & CPM – crashing of project network - complexity of project scheduling with limited resources - resource allocation - resource leveling – resource smoothing – overview of project management software.

Total Hours: 45

REFERENCES:

1. Projects: Planning, Analysis, Financing, Implementation and Review, Prasanna Chandra, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2004.
2. Project Management and Control, Narendra Singh, Himalaya Publishing, New Delhi, 2015.
3. A Management Guide to PERT/CPM, Jerome, D. Weist and Ferdinand K. Levy, Prentice Hall of India, New Delhi, 1994.

OUTCOMES:

On successfully completing this course, the student will be able to:

- Evaluate & select a project as well as develop a project profile.
- Identify various risks associated with the project and manage it effectively.
- Prepare a detailed project plan addressing its components.
- Perform technical analysis for effective project implementation
- Apply project management techniques for maximizing resource utilization.

GEDY 102 SOCIETY, TECHNOLOGY & SUSTAINABILITY

L	T	P	C
3	0	0	3

OBJECTIVES:

- To aware of new technologies through advances in Science and Engineering.
- To make them realise the profound impact on society.
- To understand the ethical issues raised by technological changes and its effect on society.
- To introduce students a broad range of perspectives on the adoption and use of technologies.
- To make them realize the need of sustainability in the context of emerging technologies.

MODULE I TECHNOLOGY AND ITS IMPACTS 09

Origin and evolution of technologies – Nature of technology- Innovation – Historical Perspective of technology – Sources of technological change - Co-evolution of technology and economy – Scientific knowledge and technological advance – Science and Engineering aspects of Technology – Impact on the Society – Social and Ethical Issues associated with technological change – Social and environmental consequences - Impact of technological change on human life –Technology and responsibility – Technology and social justice.

MODULE II TECHNOLOGY AND ITS ADVANCEMENT 09

Sociological aspects of technology – Ethics and technology – Technology and responsibility – International Economics, Globalisation and Human Rights – Sustainability and Technology – Population and environment - Technology, Energy and Environment – Organisations and technological change.

MODULE III SOCIETY AND TECHNOLOGY 09

Impact of technologies on contemporary society – Role of society in fostering the development of technology – Response to the adaption and use of technology – Impact of technology on developer and consumers – Technological change and globalisation.

MODULE IV IMPACT OF A SPECIFIC TECHNOLOGY ON HUMAN WELFARE 09

Impact of the following technologies on Human life – Medical and Biomedical – Genetics Technology – Electronics and Communications – Electronic media Technology – Information Systems Technology – Nanotechnology – Space Technology and Energy Technology.

MODULE V THE IMPORTANCE OF SUSTAINABILITY 09

Sustainability – A brief history – Concepts and contexts for sustainability – Ecological imbalance and biodiversity loss – Climate change – Population explosion. Industrial ecology – systems approach to sustainability – Green engineering and technology-sustainable design- sustainable manufacturing-Green consumer movements – Environmental ethics – Sustainability of the planet Earth – Future planning for sustainability.

Total Hours: 45

REFERENCES:

1. Volti Rudi, “Society and Technology Change”, 6th Edition, Worth publishers Inc, USA, 2009.
2. Arthur W.A, “The nature of Technology: What it is and how it evolves”, Free Press, NY, USA, 2009.
3. Winston M and Edelbach R, “Society, Ethics and Technology”, 3rd Edition, San Francisco, USA, 2005.
4. Martin A.A Abraham, “Sustainability Science and Engineering: Defining Principles”, Elsevier Inc, USA, 2006.
5. R.V.G.Menon, “Technology and Society”, Pearson Education, India, 2011.

OUTCOMES:

At the end of this course, the students will be able to

- Understand the benefits of modern technology for the well-being of human life.
- Connect sustainability concepts and technology to the real world challenges.
- Find pathway for sustainable society.

GEDY 103	ARTIFICIAL INTELLIGENCE	L	T	P	C
		3	0	0	3

OBJECTIVES:

- Expose the history and foundations of artificial intelligence.
- Showcase the complexity of working on real time problems underlying the need for intelligent approaches.
- Illustrate how heuristic approaches provide a good solution mechanism.
- Provide the mechanisms for simple knowledge representation and reasoning.
- Highlight the complexity in working with uncertain knowledge.
- Discuss the current and future applications of artificial intelligence.

MODULE I HISTORY AND FOUNDATIONS 08

History – Scope – Influence from life – Impact of computing domains - Agents in environments - Knowledge representation – Dimensions of Complexity – Sample application domains – Agent structure.

MODULE II SEARCH 10

Problem solving as search – State spaces – Uninformed Search – Heuristic search – Advanced search – Constraint satisfaction - Applications.

MODULE III KNOWLEDGE REPRESENTATION AND REASONING 10

Foundations of knowledge representation and reasoning, representing and reasoning about objects, relations, events, actions, time, and space predicate logic, situation calculus, description logics, reasoning with defaults, reasoning about knowledge, sample applications.

MODULE IV REPRESENTING AND REASONING WITH UNCERTAIN KNOWLEDGE 08

Probability, connection to logic, independence, Bayes rule, Bayesian networks, probabilistic inference, sample applications.

MODULE V CASE STUDY AND FUTURE APPLICATIONS 09

Design of a game/Solution for problem in student's domain. Natural Language processing, Robotics, Vehicular automation – Scale, Complexity, Behaviour – Controversies.

Total Hours: 45

TEXT BOOK:

1. Stuart Russell and Peter Norvig, Artificial Intelligence: A Modern Approach, Prentice Hall, Third Edition, 2010.
2. David Poole, Alan Mackworth, Artificial Intelligence: Foundations of Computational Agents, Cambridge University Press, 2010.
3. Nils J. Nilsson, The Quest for Artificial Intelligence, Cambridge University Press, Online edition, 2013.
4. Keith Frankish, William M. Ramsey (eds) The Cambridge Handbook of Artificial Intelligence, Cambridge University Press, 2014.

OUTCOMES:

Students who complete this course will be able to

- Discuss the history, current applications, future challenges and the controversies in artificial intelligence.
- Apply principle of AI in the design of an agent and model its actions.
- Design a heuristic algorithm for search problems.
- Analyze and represent the fact using logic for a given scenario
- Represent uncertainty using probabilistic models
- Develop a simple game or solution using artificial intelligence techniques.

GEDY 104 GREEN COMPUTING L T P C
3 0 0 3

OBJECTIVES:

- To focus on the necessity of green computing technology.
- To expose to various issues with information technology and sustainability.
- To attain knowledge on the technologies for enabling green cloud computing.
- To elaborate on the energy consumption issues
- To illustrate a Green and Virtual Data Center
- To develop into a Green IT Technologist.

MODULE I INTRODUCTION 08

Trends and Reasons to Go Green - IT Data Center Economic and Ecological Sustainment - The Growing Green Gap: Misdirected Messaging, Opportunities for Action - IT Data Center “Green” Myths and Realities - PCFE Trends, Issues, Drivers, and Related Factors - Green Computing and Your Reputation- Green Computing and Saving Money- Green Computing and the Environment

MODULE II CONSUMPTION ISSUES 10

Minimizing power usage – Cooling - Electric Power and Cooling Challenges - Electrical – Power -Supply and Demand Distribution - Determining Energy Usage - From Energy Avoidance to Efficiency - Energy Efficiency Incentives, Rebates, and Alternative Energy Sources - PCFE and Environmental Health and Safety Standards- Energy-exposed instruction sets- Power management in power-aware real-time systems.

MODULE III NEXT-GENERATION VIRTUAL DATA CENTERS 09

Data Center Virtualization - Virtualization beyond Consolidation - Enabling Transparency - Components of a Virtual Data Center - Datacenter Design and Redesign - Greening the Information Systems - Staying Green- Building a Green Device Portfolio- Green Servers and Data Centers- Saving Energy

MODULE IV TECHNOLOGIES FOR ENABLING GREEN AND VIRTUAL DATA CENTERS 08

Highly Effective Data Center Facilities and Habitats for Technology - Data Center Electrical Power and Energy Management - HVAC, Smoke and Fire Suppression - Data Center Location - Virtual Data Centers Today and Tomorrow - Cloud Computing, Out-Sourced, and Managed Services.

MODULE V SERVERS AND FUTURE TRENDS OF GREEN COMPUTING 10

Server Issues and Challenges - Fundamentals of Physical Servers - Types, Categories, and Tiers of Servers - Clusters and Grids - Implementing a Green and Virtual Data Center - PCFE and Green Areas of Opportunity- 12 Green Computer Companies- What's in Green computer science-Green off the Grid aimed for data center energy evolution-Green Grid Consortium- Green Applications- Green Computing Making Great Impact On Research

Total Hours: 45

REFERENCES:

1. Bud E. Smith,"Green Computing Tools and Techniques for Saving Energy, Money, and Resources", Taylor & Francis Group, CRC Press, ISBN-13: 978-1-4665-0340-3, 2014.
2. Jason Harris, "Green Computing and Green IT Best Practices, On Regulations and Industry Initiatives, Virtualization and power management, materials recycling and Tele commuting, Emereo Publishing .ISBN-13: 978-1-9215-2344-1,2014.
3. Ishfaq Ahmed & Sanjay Ranka, "Handbook of Energy Aware and Green Computing", CRC Press, ISBN: 978-1-4665-0116-4, 2013.
4. Kawahara, Takayuki, Mizuno, "Green Computing with Emerging Memory", Springer Publications, ISBN:978-1-4614-0811-6, 2012
5. Greg Schulz, "The Green and Virtual Data Center", CRC Press, ISBN-13:978-1-4200-8666-9, 2009.
6. Marty Poniatowski, "Foundation of Green IT: Consolidation, Virtualization, Efficiency, and ROI in the Data Center", Printice Hall, ISBN: 9780-1-3704-375-0, 2009.

OUTCOMES:

Students who complete this course will be able to

- Demonstrate issues relating to a range of available technologies, systems and practices to support green computing.
- Select appropriate technologies that are aimed to reduce energy consumption.

- Address design issues needed to achieve an organizations' green computing objectives.
- Analyze the functionality of Data Centers.
- Critically evaluate technologies and the environmental impact of computing resources for a given scenario.
- Compare the impact of Green Computing with other computing techniques.

GEDY 105 GAMING DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To master event-based programming
- To learn resource management as it relates to rendering time, including level-of-detail and culling.
- To become familiar with the various components in a game or game engine.
- To explore leading open source game engine components.
- To become familiar of game physics.
- To be compatible with game animation.

MODULE I INTRODUCTION 09

Magic Words–What Skills Does a Game Designer Need? –The Most Important Skill - The Five Kinds of Listening-The Secret of the Gifted.

MODULE II THE DESIGNER CREATES AN EXPERIENCE 09

The Game Is Not the Experience -Is This Unique to Games? -Three Practical Approaches to Chasing Rainbows -Introspection: Powers, Perils, and Practice - Dissect Your Feelings -Defeating Heisenberg -Essential Experience.

MODULE III THE EXPERIENCE IN THE PLAYER MIND AND GAME MECHANICS 08

Modeling – Focus -Empathy –Imagination –Motivation – Space – Objects, Attributes, and States – Actions – Rules.

MODULE IV GAMES THROUGH AN INTERFACE 09

Breaking it Down –The Loop of Interaction – Channels of Information – Other Interface.

MODULE V BALANCED GAME MECHANICS 10

Balance –The Twelve Most Common Types of Game Balance –Game Balancing Methodologies - Balancing Game Economies.

Total Hours: 45

REFERENCES:

1. Jesse Schell, "The Art of Game Design: A Book of Lenses", 2nd Edition ISBN-10: 1466598646, 2014.
2. Ashok Kumar, Jim Etheredge, Aaron Boudreaux, “Algorithmic and Architectural Gaming Design: Implementation and Development", 1st edition, Idea Group, U.S ISBN-10: 1466616342, 2012.
3. Katie SalenTekinba, Melissa Gresalfi, Kylie Peppler, Rafi Santo, "Gaming the System - Designing with Gamestar Mechanic" MIT Press , ISBN-10: 026202781X, 2014.
4. James M. Van Verth, Lars M. Bishop "Essential Mathematics for Games and Interactive Applications", Third Edition,A K Peters/CRC Press, ISBN-10: 1482250926, 2015.

OUTCOMES:

Students who complete this course will be able to

- Realize the basic history and genres of games
- Demonstrate an understanding of the overall game design process
- Explain the design tradeoffs inherent in game design
- Design and implement basic levels, models, and scripts for games
- Describe the mathematics and algorithms needed for game programming
- Design and implement a complete three-dimensional video game

GEDY 106 SOCIAL COMPUTING

L	T	P	C
3	0	0	3

OBJECTIVES:

- To create original social applications, critically applying appropriate theories and effective practices in a reflective and creative manner.
- To critically analyze social software in terms of its technical, social, legal, ethical, and functional features or affordances.
- To encourage the development of effective communities through the design, use, and management of social software.
- To give students with a base of knowledge and advances for them to critically examine existing social computing services.
- To plan and execute a small-scale research project in social computing in a systematic fashion.
- To become familiar with the concept of computational thinking.

MODULE I BASIC CONCEPTS 09

Networks and Relations: Relations and Attributes, Analysis of Network Data, Interpretation of network data -New Social Learning – Four Changes that Shift Work - Development of Social Network Analysis: Sociometric analysis and graph theory, Interpersonal Configurations and Cliques – Analysing Relational Data.

MODULE II SOCIAL LINK 09

Individual Actors, Social Exchange Theory, Social Forces, Graph Structure, Agent Optimization Strategies in Networks – Hierarchy of Social Link Motivation- Social Context.

MODULE III SOCIAL MEDIA 08

Trends in Computing – Motivations for Social Computing – Social Media: Social relationships, Mobility and Social context – Human Computation – Computational Models- Business use of social Media.

MODULE IV SOCIAL INFORMATION FILTERING 09

Mobile Location Sharing – Location based social media analysis – Social Sharing and Social Filtering – Automated recommender Systems – Traditional and Social Recommender Systems.

MODULE V SOCIAL NETWORK STRATEGY 10

Application of Topic Models – Opinions and Sentiments – Recommendation Systems – Language Dynamics and influence in online communities – Psychometric analysis – Case Study: Social Network Strategies for surviving the zombie apocalypse.

Total Hours: 45

REFERENCES:

1. Tony Bingham, Marcia Conner, “The New Social Learning, Connect. Collaborate. Work”, 2nd Edition, ATD Press, ISBN-10:1-56286-996-5, 2015.
2. Nick Crossley, Elisa Bellotti, Gemma Edwards, Martin G Everett, Johan Koskinen, Mark Tranmer, “Social Network Analysis for Ego-Nets”, SAGE Publication, 2015.
3. Zafarani, Abbasi and Liu, Social Media Mining: An Introduction, Cambridge University Press, 2014.
4. Christina Prell, “Social Network Analysis: History, Theory and Methodology”, 1st Edition, SAGE Publications Ltd, 2012.
5. John Scott, “Social Network Analysis”, Third Edition,SAGE Publication, 2013.
6. Jennifer Golbeck, “Analyzing the Social Web”, Elsevier Publication, 2013.
7. Huan Liu, John Salerno, Michael J. Young, “Social computing and Behavioral Modeling”, Springer Publication, 2009.

OUTCOMES:

Students who complete this course will be able to

- Realize the range of social computing applications and concepts.
- Analyze data left after in social media.
- Recognize and apply the concepts of computational models underlying social computing.
- Take out simple forms of social diagnostics, involving network and language models, applying existing analytic tools on social information.
- Evaluate emerging social computing applications, concepts, and techniques in terms of key principles.
- Design and prototype new social computing systems.

GEDY 107	SOFT COMPUTING	L	T	P	C
		3	0	0	3

OBJECTIVES:

The aim of the course is to

- Enumerate the strengths and weakness of soft computing
- Illustrate soft computing methods with other logic driven and statistical method driven approaches
- Focus on the basics of neural networks, fuzzy systems, and evolutionary computing
- Emphasize the role of euro-fuzzy and hybrid modeling methods
- Trace the basis and need for evolutionary computing and relate it with other soft computing approaches

MODULE I SOFT COMPUTING - BASICS 06

Soft computing – Hard Computing – Artificial Intelligence as the basis of soft computing – Relation with logic driven and statistical method driven approaches- Expert systems – Types of problems: Classification, Functional approximation, Optimizations – Modeling the problem – Machine Learning – Hazards of Soft Computing – Current and future areas of research

MODULE II ARTIFICIAL NEURAL NETWORK 12

Artificial Neuron – Multilayer perceptron – Supervised learning – Back propagation network –Types of Artificial Neural Network: Supervised Vs Un Supervised Network – Radial basis function Network – Self Organizing Maps – Recurrent Network – Hopfield Neural Network – Adaptive Resonance Theory – Issues in Artificial Neural Network – Applications

MODULE III FUZZY SYSTEMS 09

Fuzzy Logic – Membership functions – Operators – Fuzzy Inference systems – Other sets: Rough sets, Vague Sets – Fuzzy controllers - Applications

MODULE IV NEURO FUZZY SYSTEMS 09

Cooperative Neuro fuzzy systems – Neural network driven fuzzy reasoning – Hybrid Neuro fuzzy systems – Construction of Neuro Fuzzy systems: Structure Identification phase, Parameter learning phase – Applications

MODULE V EVOLUTIONARY COMPUTING 09

Overview of evolutionary computing – Genetic Algorithms and optimization – Genetic Algorithm operators – Genetic algorithms with Neural/Fuzzy systems – Variants of Genetic Algorithms– Population based incremental learning – Evolutionary strategies and applications

Total Hours: 45

TEXTBOOKS:

1. Samir Roy, “Introduction to Soft Computing: Neuro-Fuzzy and Genetic Algorithms”, Pearson, 2013
2. Anupam Shukla, Ritu Tiwari and Rahul Kala, “Real life applications of Soft Computing”, CRC press, 2010.
3. Fakhreddine O. Karray, “Soft Computing and Intelligent Systems Design: Theory, Tools and Applications”, Pearson, 2009

OUTCOMES:

At the end of the course the students will be able to

- Enumerate the theoretical basis of soft computing
- Explain the fuzzy set theory
- Discuss the neural networks and supervised and unsupervised learning networks
- Demonstrate some applications of computational intelligence
- Apply the most appropriate soft computing algorithm for a given situation

GEDY 108 EMBEDDED SYSTEM PROGRAMMING

L	T	P	C
3	0	0	3

OBJECTIVES:

- To introduce the design of embedded computing systems with its hardware and software architectures.
- To describe entire software development lifecycle and examine the various issues involved in developing software for embedded systems.
- To analyze the I/O programming and Embedded C coding techniques
- To equip students with the software development skills necessary for practitioners in the field of embedded systems.

MODULE I INTRODUCTION OF EMBEDDED SYSTEM 09

Embedded computing –characteristics and challenges –embedded system design process –Overview of Processors and hardware units in an embedded system – Compiling, Linking and locating – downloading and debugging –Emulators and simulators processor – External peripherals – Memory testing – Flash Memory.

MODULE II SOFTWARE TECHNOLOGY 09

Software Architectures, Software development Tools, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance.

MODULE III INPUT/OUTPUT PROGRAMMING 09

I/O Instructions, Synchronization, Transfer Rate & Latency, Polled Waiting Loops, Interrupt – Driven I/O, Writing ISR in Assembly and C, Non Maskable and Software Interrupts

MODULE IV DATA REPRESENTATION IN EMBEDDED SYSTEMS 09

Data representation,Twos complement, Fixed point and Floating Point Number Formats,Manipulating Bits in -Memory, I/O Ports, Low level programming in C,Primitive data types, Arrays, Functions,Recursive Functions, Pointers, Structures & Unions,Dynamic Memory Allocation,File handling,Linked lists, Queues, Stacks.

MODULE V EMBEDDED C 09

Embedded Systems programming in C – Binding & Running Embedded C program in Keil IDE – Dissecting the program -Building the hardware. Basic techniques for

reading & writing from I/O port pins – switch bounce - LED Interfacing using Embedded C.

Total Hours: 45

REFERENCES:

1. Marilyn Wolf, "Computers as components ", Elsevier, 2012.
2. Qing Li and Carolyn Yao, "Real-Time Concepts for Embedded Systems", CMP Books, 2003.
3. Daniel W.Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education
4. Michael Bass, "Programming Embedded Systems in C and C++", Oreilly, 2003.

OUTCOMES:

On completion of this course the student will be able to

- Design the software and hardware components in embedded system
- Describe the software technology
- Use interrupt in effective manner
- Use keil IDE for programming
- Program using embedded C for specific microcontroller
- Design the embedded projects

GEDY 109 PRINCIPLES OF SUSTAINABLE DEVELOPMENT

L	T	P	C
3	0	0	3

OBJECTIVES:

- To impart knowledge in the concepts and dimensions of sustainable development.
- To gain knowledge on the framework for achieving sustainability.

MODULE I CONCEPT OF SUSTAINABLE DEVELOPMENT 09

Environment and Development - Population poverty and Pollution –Global and Local environmental issues –Resource Degradation- Greenhouse gases –Desertification-industrialization –Social insecurity, Globalization and environment. History and emergence of the concept of sustainable development-Objectives of Sustainable Development.

MODULE II COMPONENTS AND DIMENSIONS OF SUSTAINABLE DEVELOPMENT 09

Components of Sustainability –Complexity of growth and equity – Social economic and environmental dimensions of sustainable development – Environment– Biodiversity– Natural – Resources– Ecosystem integrity– Clean air and water– Carrying capacity– Equity, Quality of Life, Prevention, Precaution–Preservation and Public Participation Structural and functional linking of developmental dimensions.

MODULE III FRAMEWORK FOR ACHIEVING SUSTAINABILITY 09

Operational guidelines– interconnected prerequisites for sustainable development Empowerment of Women, children, Youth, Indigenous People, Non-Governmental Organizations Local Authorities, Business and industry–Science and Technology for sustainable development – performance indicators of sustainability and assessment mechanism– Constraints and barriers for sustainable development.

MODULE IV SUSTAINABLE DEVELOPMENT OF SOCIO ECONOMIC SYSTEMS 09

Demographic dynamics of sustainability – Policies for socio-economic development –Strategies for implementing eco-development programmes Sustainable development through trade –Economic growth –Action plan for implementing

sustainable development –Urbanization and sustainable Cities –Sustainable Energy and Agriculture –sustainable livelihoods.

MODULE V SUSTAINABLE DEVELOPMENT AND INTERNATIONAL RESPONSE 09

Role of developed countries in the development of developing countries– international summits–Stockholm to Johannesburg –Rio principles–Agenda-Conventions–Agreements– Tokyo Declaration –Doubling statement–Tran boundary issues integrated approach for resources protection and management

Total Hours: 45

REFERENCES:

1. Sayer J. and Campbell, B., The Science of Sustainable Development: Local Livelihoods and the Global environment - Biological conservation restoration & Sustainability, Cambridge university Press, London, 2003.
2. M.K. Ghosh Roy. and Timberlake, Sustainable Development, Ane Books Pvt. Ltd, 2011.
3. Mackenthun K.M., Concepts in Environmental Management, Lewis Publications London,1999.
4. APJ Abdul Kalam and Srijan Pal Singh, Target 3 Billion: Innovative Solutions Towards Sustainable Development, Penguin India, 2011

OUTCOMES:

At the end of the course the student will be able to

- Describe the concepts of sustainable development
- Define the components and dimensions of sustainable development
- Outline the Frame work for achieving sustainability.
- State the policies and strategies for implementing sustainable development for Socio economic programmes.
- Examine the role of developed countries in sustainable development.

GEDY 110	QUANTITATIVE TECHNIQUES IN MANAGEMENT	L	T	P	C
		3	0	0	3

OBJECTIVE:

To impart knowledge on

- Concepts of operations research
- Inventory control in production management
- Financial management of projects
- Decision theory and managerial economics

MODULE I OPERATIONS RESEARCH 09

Introduction to Operations research – Linear programming –Graphical and Simplex Methods, Duality and Post-Optimality Analysis –Transportation and Assignment Problems

MODULE II PRODUCTION MANAGEMENT 09

Inventory control, EOQ, Quantity Discounts, Safety Stock– Replacement Theory – PERT and CPM – Simulation Models –Quality Control.

MODULE III FINANCIAL MANAGEMENT 09

Working Capital Management–Compound Interest and Present Value methods– Discounted Cash Flow Techniques–Capital Budgeting.

MODULE IV DECISION THEORY 09

Decision Theory–Decision Rules–Decision making under conditions of certainty, risk and uncertainty–Decision trees–Utility Theory.

MODULE V MANAGERIAL ECONOMICS 09

Cost concepts–Breakeven Analysis–Pricing techniques–Game Theory applications.

Total Hours: 45

REFERENCES:

1. Vohra, N.D. , Quantitative Techniques in Management, Tata McGraw Hill Co., Ltd, New Delhi, 2009.
2. Seehroeder, R.G., Operations Management, McGraw Hill, USA, 2002.

3. Levin, R.I, Rubin, D.S., and Stinsonm J., Quantitative Approaches to Management, McGraw Hill Book Co., 2008.
4. Frank Harrison, E., The Managerial Decision Making Process, Houghton Miffin Co. Boston, 2005.
5. Hamdy A. Taha, Operations Research- An Introduction, Prentice Hall, 2002.

OUTCOMES:

At the end of the course, the students will be able to

- Apply the concepts of operations research for various applications
- Create models for inventory control in production management
- Compute the cash flow for a project
- Choose a project using decision theory based on the risk criterion.
- Apply the concepts of managerial economics in construction management

GEDY 111 PROGRAMMING USING MATLAB & SIMULINK

L	T	P	C
1	0	2	2

OBJECTIVES:

The aim of this course is to:

- Teach students how to mathematically model engineering systems
- Teach students how to use computer tools to solve the resulting mathematical models. The computer tool used is MATLAB and the focus will be on developing and solving models of problems encountered in engineering fields

MODULE I INTRODUCTION TO MATLAB AND DATA PRESENTATION 10

Introduction to MATLAB-Vectors, Matrices -Vector/Matrix Operations & Manipulation-Functions vs scripts- Making clear and compelling plots-Solving systems of linear equations numerically and symbolically.

Lab Experiments

1. Study of basic matrix operations and manipulations.
2. Numerical and symbolical solution of linear equations.

MODULE II ROOT FINDING AND MATLAB PLOT FUNCTION 10

Linearization and solving non-linear systems of equations- The Newton-Raphson method- Integers and rational numbers in different bases- Least squares regression - Curve fitting-Polynomial fitting and exponential fitting.

Lab Experiments

1. Solution of non linear equations using Newton-Raphson method.
2. Determination of polynomial fit and exponential fit for the given data.

MODULE III LINEAR AND NON-LINEAR DIFFERENTIAL EQUATIONS 13

Numerical integration and solving first order, ordinary differential equations (Euler's method and Runge-Kutta)- Use of ODE function in MATLAB- Converting second order and higher ODEs to systems of first order ODEs- Solving systems of higher order ODEs via Euler's method and Runge-Kutta)- Solving single and systems of non-linear differential equations by linearization-Use of the function ODE in MATLAB to solve differential equations - Plot Function –Saving & Painting Plots.

Lab Experiments

1. Solution of fourth order linear differential equations using
    a. Trapezoidal Rule

b. Euler method

2. Solution of fourth order non-linear differential equations using
    a. Modified Euler method
    b. Runge – Kutta method

MODULE IV INTRODUCTION OF SIMULINK 12

Simulink & its relations to MATLAB – Modeling a Electrical Circuit- Modeling a fourth order differential equations- - Representing a model as a subsystem- Programme specific Simulink demos.

Lab Experiments

1. Solution of fourth order non-linear differential equations using simulink.
2. Programme specific experiment based on simulink.

Total Hours (Including Practicals): 45

REFERENCE:

1. Griffiths D V and Smith I M, “Numerical Methods for Engineers”, Blackwell, 1991.
2. LaureneFausett, “Applied Numerical Analysis Using MATLAB”, Pearson 2008.
3. Moin P, “Fundamentals of Engineering Numerical Analysis”, Cambridge University Press, 2001.
4. Wilson HB, Turcotte LH, Advanced mathematics and mechanics applications using MATLAB”, CRC Press, 1997
5. Ke Chen, Peter Giblin and Alan Irving, “Mathematical Exploration with MATLAB”, Cambridge University Press, 1999.

OUTCOMES:

At the end of this unit students will be able to:

- Use Matlab as a convenient tool for solving a broad range of practical problems in engineering from simple models to real examples.
- Write programs using first principles without automatic use of built-in ones.
- Write programs for solving linear and nonlinear systems, including those arising from boundary value problems and integral equations, and for root-finding and interpolation, including piecewise approximations.
- Be fluent in exploring Matlab’s capabilities, such as using matrices as the fundamental data-storage unit, array manipulation, control flow, script and function m-files, function handles, graphical output.

- Make use of Maltab visual capabilities for all engineering applications.
- An ability to identify, formulate, and solve engineering problems. This will be accomplished by using MATLAB to simulate the solution to various problems in engineering fields

GEDY 112 JAVA PROGRAMMING

L	T	P	C
3	0	0	3

OBJECTIVES:

- To study the syntax and necessity of decision making and iterative statements.
- To create a class and invoke the methods with ability handle abnormal conditions.
- To learn to work with various string methods and collection framework.
- To establish a connection to database from java application.
- To understand why Java is useful for the designing web applications.
- To design a graphical user interface (GUI) with Java Swing.

MODULE I INTRODUCTION TO JAVA PROGRAMMING 06

History and Evolution of Java – Overview of Java – Data types, variables and arrays – Operators – Control statements.

MODULE II METHODS AND CLASSES 08

Class fundamentals – Declaring objects – Methods – Constructors – Garbage collection – Overloading methods – Constructor overloading – Access control – Inheritance – Packages - Exception handling.

MODULE III STRING HANDLING AND COLLECTIONS 07

String Handling - Special String Operations - String Literals- String Conversion - Collections Overview - The Collection Interfaces -The Collection Classes - Accessing a collection Via an Iterator - Working With Maps, Comparators.

MODULE IV DATABASE CONNECTIVITY 08

JDBC - JDBC Driver Types - JDBC Packages - Database Connection - Associating the JDBC/ODBC Bridge with the Database - Statement Objects – Result Set - Transaction Processing – Metadata - Exceptions.

MODULE V SERVER PROGRAMMING 09

The Life Cycle of a Servlet - Using Tomcat for Servlet Development -The Servlet API - Handling HTTP Requests and Responses - Using Cookies - Session Tracking - Java Server Pages (JSP)-Session Objects

MODULE VI SWING PROGRAMMING 07

Concepts of Swing - Java Foundation Class (JFC) - Swing Packages and Classes - Working with Swing - Swing Components

L – 45; TOTAL HOURS-45

REFERENCES :

1. Herbert Schildt, “Java The Complete Reference”, 11th Edition, McGraw Hill, 2018, ISBN: 9781260440249.
2. Joshua Bloch , “Effective Java Paperback”,3rd Edition, Addison Wesley,2017,ISBN: 978-0134685991.
3. E Balagurusamy, “Programming with Java”, 6th Edition, Tata Mcgraw Hill, 2019,ISBN: 978-9353162344.

OUTCOMES:

Students who complete this course will be able to

- Understand the fundamentals java programming language
- Use the Java programming language for various programming technologies.
- Perform various string operations on any given text from user.
- Connect any database with java program and manipulate the contents.
- Write a server side programming which can evaluate the input and respond to user request
- Develop user interface using java swings.

GEDY 113 PYTHON PROGRAMMING

L	T	P	C
3	0	0	3

OBJECTIVES :

- To study the control statements and string functions of python.
- To practice python data structures - lists, tuples, dictionaries.
- To organize input/output with files in Python.
- To learn the python tools as well as Unicode process.
- To explore advance python including decorators and metaclasses.
- To integrate python with embedded systems.

MODULE I INTRODUCTION TO PYTHON PROGRAMMING 07

Installation and environment set up – syntax used in python – variable types – operators – Loops – decision making – string functions - recursion - GUI basics.

MODULE II LISTS, TUPLES AND DICTIONARIES 08

Lists - list operations - list slices - list methods - list loop – mutability- aliasing - cloning lists - list parameters - Tuples: tuple assignment- tuple as return value- Dictionaries- operations and methods- advanced list processing - list comprehension- selection sort - insertion sort- merge sort- histogram.

MODULE III FILES, MODULES AND PACKAGES 08

Files and exception - text files - reading and writing files - format operator - command line arguments - errors and exceptions - handling exceptions – modules – packages - word count- copy file.

MODULE IV UNICODE AND BYTE STRINGS 07

String basics - coding basic strings –coding Unicode strings- 3.X bytes objects- 3.X/2.6+ byte array object- text and binary files – Unicode files

MODULE V DECORATORS AND METACLASS 08

Decorator basics- coding function decorators- coding class decorators – managing functions and classes –the metaclass model- declaring metaclasses-coding metaclasses-inheritance and instance-metaclass methods

MODULE VI EMBEDDED PROGRAMMING USING PYTHON 07

Web interface – system tools – script execution context - Motion-triggered LEDs – Python - Arduino prototyping-storing and plotting Arduino data-Remote home monitoring system.

L – 45; Total Hours : 45

REFERENCES :

1. Guido van Rossum and Fred L. Drake Jr, “An Introduction to Python – Revised and updated for Python 3.2, Network Theory Ltd., 2011.
2. Allen B. Downey, ``Think Python: How to Think Like a Computer Scientist‘‘, 2nd edition, Updated for Python 3, Shroff/O‘Reilly Publishers, 2016, ISBN-13:978-1491939369.
3. Nick Goddard, “Python Programming”, 2nd edition, ISBN: 1533337772, 2016.
4. Mark Lutz, Learning Python: Powerful Object-Oriented Programming, 5th Edition, O'Reilly Media, 2013.
5. Pratik Desai, “Python Programming for Arduino”, 1st edition, Packt publishing, 2015, ISBN: 9781783285938.
6. Richard H. Barnett, Sarah Cox, Larry O'Cull, “Embedded C Programming and the Atmel AVR”, 2nd edition, 2006.
7. Michael Barr, Anthony Massa, “Programming Embedded Systems”, 2nd Edition, O'Reilly Media, 2006.

OUTCOMES :

Students to complete this course will be able to

- Implement date and time function programming using python.
- Represent compound data using Python lists, tuples, dictionaries
- Read and write data from/to files in Python Programs.
- Instrument the unicode process using python tools
- Build advance python programs using decorators and metaclass.
- Develop embedded system with python programming.

GEDY 114 INTELLECTUAL PROPERTY RIGHTS (IPR)

L	T	P	C
1	0	0	1

OBJECTIVES:

- To study about Intellectual property rights and its need
- To explore the patent procedure and related issues

MODULE I INTRODUCTION 07

Introduction and the need for intellectual property right (IPR) –IPR in India – Genesis and Development – IPR in abroad – Important examples of IPR– Copyrights, Trademarks, Patents, Designs, Utility Models, Trade Secrets and Geographical Indications – Industrial Designs

MODULE II PATENT 08

Concept of Patent – Product / Process Patents & Terminology– Duration of Patents – Law and Policy Consideration Elements of Patentability –- Patentable Subject Matter– Procedure for Filing of Patent Application and types of Applications – Procedure for Opposition – Revocation of Patents – Working of Patents- Patent Agent– Qualification and Registration Procedure – Patent databases and information system – Preparation of patent documents – Process for examination of patent application- Patent infringement– Recent developments in patent system

Total Hours: 15

REFERENCES

1. B.L.Wadehra; Law Relating to Patents, Trade Marks, Copyright, Designs & Geographical Indications; Universal law Publishing Pvt. Ltd., India 2000
2. AjitParulekar and Sarita D' Souza, Indian Patents Law – Legal & Business Implications; Macmillan India ltd , 2006
3. P. Narayanan; Law of Copyright and Industrial Designs; Eastern law House, Delhi, 2010.
4. E. T. Lokganathan, Intellectual Property Rights (IPRs): TRIPS Agreement & Indian Laws Hardcover, 2012
5. Alka Chawla, P N Bhagwati , Law of Copyright Comparative Perspectives 1st Edition, LexisNexis, 2013

6. V. K. Ahuja, Law Relating to Intellectual Property Rights 2nd Edition, LexisNexis, 2nd Edition, 2013
7. Deborah E. Bouchoux, Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 2015
8. Jatindra Kumar Das, Law of Copyright, PHI Learning, 2015

OUTCOMES:

Students should be able to

- Identify the various types of intellectual property and their value
- Apply the procedure to file a patent and to deal the related issues
- Search and extract relevant information from various intellectual database